Honeywell

FIELD ENGINEERING

SERIES 16 - 5081 PAPER TAPE READER/PUNCH CONTROLLER THEORY OF OPERATION MANUAL

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CONTENTS

CONTENTS (CONTINUED)

ILLUSTRATIONS

TABLES

SECTION 1
GENERAL DESCRIPTION

INTRODUCTION

The Series 16-5081 Paper Tape Reader/Punch Controller (PTRPC) Option consists of a 1 x 3μ - BLOC Assembly of interface logic which links the Main Frame of an H316 or DDP-416/516 General Purpose Computer to the 16-5082 Paper Tape Reader Option and/or the 16-5085 Facit 4070 Low Speed Paper Tape Punch Option. The 16-5081 PTRPC comprises four committed logic μ-PACs which were designed specifically for this option.

In addition to the units described previously it is also possible to control the 16-5086 Facit 4060 High Speed Paper Tape Punch/Honeywell Electronic Unit combination, with the 16-5081 PTRPC option, by inclusion of the additional eight standard μ-PACs contained in the 16-5086 option.

A choice of two options of Paper Tape Reader Slow Speed Paper Tape Punch and High Speed Paper Tape Punch is available. The complete list of options is shown below:

Honeywell Paper Tape Reader :

16-5082; Table Top Model

16-5083; Rack-Mounted

Facit 4070 Paper Tape Punch:

16-5085; Table Top Model

16-5084; Rack-Mounted

Facit 4060 Paper Tape Punch:

16-5086; Table Top Model

16-5087; Rack-Mounted

OUTLINE OF OPERATION

A block diagram of the PTRPC is shown in Figure 1-1. Data is transferred to the Central Processor from the Paper Tape Reader or from the Central Processor to the Paper Tape Punch under program control. One frame of data at a time (up to 8 bits per

frame) may be read into the controller and transferred to the computer 'A' register, via the input bus lines, or transferred from the Central Processor via the output bus lines to the controller and punched onto paper tape.

INTERFACE LOGIC MODULE

The interface logic module (contained in a 1 x 3μ-BLOC) provides the logic necessary to decode commands from the computer and generate the signals necessary to control the transfer of data from the Paper Tape Reader to the Central Processor or from the Central Processor to the Paper Tape Punch.

The μ-PAC complement and module content description of the four newly designed committed logic PACs and the eight additional PACs, contained in the High Speed Punch option, are given in Tables 1-1 and 1-2 respectively.

The printed circuit board assembly layouts for the four newly designed committed logic PACs are shown in LBD No. EO84.

PERFORMANCE SPECIFICATIONS

Speed

16-5082/3 Honeywell Paper Tape Reader; 300 char/sec.

16-5084/5 Facit 4070 Slow Speed Punch; 75 char/sec.

16-5086/7 Facit 4060 High Speed Punch; 150 char/sec.

Braking (Reader)

Braking distances are affected by the condition of the tape. At best the reader will halt on the character just read. At worst (e.g. thick splice just passing the brake) the reader will stop before the next character to be read.

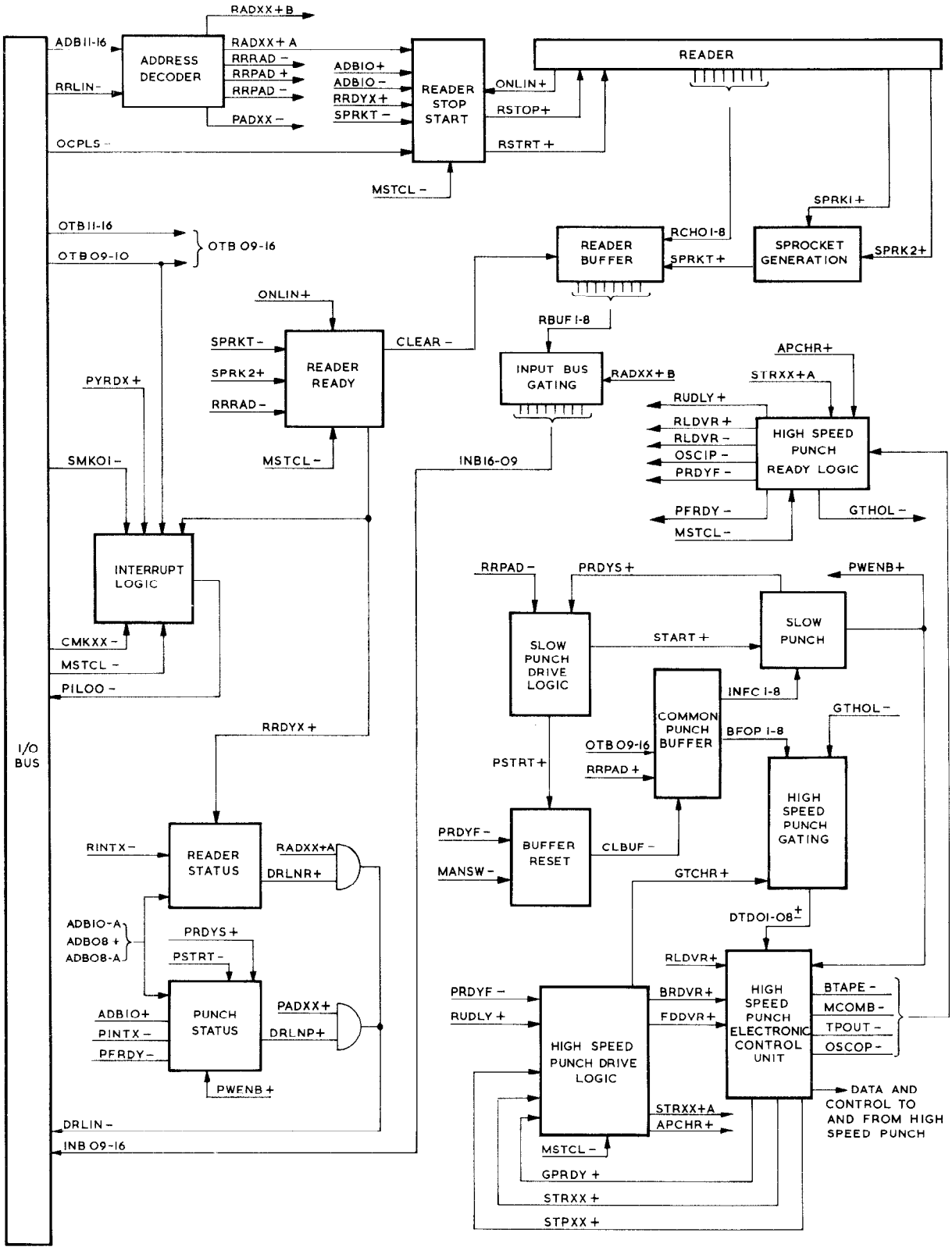


Figure 1-1 Interface Block Diagram

TABLE 1-1

BASIC 16-5081 μ-PAC COMPLEMENT

PAC	NUMBER USED	FUNCTION	IC TYPE	COMPRISING NUMBER	COMPRISING TYPE
NC026	1	Address Decoding	830	1	Dual four I/P NAND
		and Peripheral	836	3	Sext single I/P NAND
		Status	846	3	Quad. two I/P NAND
			848	2	JK or RS Flip-Flop
			862	1	Triple three I/P NAND
			SN 7401	1	Quad. two I/P NAND
NC028	1	Reader Start/Stop,	832	1	Dual four I/P Buffer
		Sprocket, Ready and	836	1	Sext. single I/P NAND
		Buffer	846	8	Quad. two I/P NAND
			848	1	JK or RS Flip-Flop
			862	1	Triple three I/P NAND
			SN 4701	2	Quad. two I/P NAND
NC029	1	Punch Buffer	832	4	Dual four I/P Buffer
			846	6	Quad. two I/P NAND
NC030	1	High Speed Punch	832	1	Dual four I/P Buffer
		Start/Stop and	846	4	Quad. two I/P NAND
		Character Gating.	848	3	JK or RS Flip-Flop
		Low Speed Punch	862	1	Triple three I/P NAND
		Start/Stop.			

Note: All 800 series I.C.'s mentioned have 900 series equivalents which may be used as direct replacements. (e.g. 832 exchangeable with 932). The SN 7401 I.C.'s may be directly replaced with F32 I.C.'s.

TABLE 1-2

ADDITIONAL μ-PACs REQUIRED FOR HIGH SPEED PUNCH

PAC	NUMBER USED	TYPE	COMPRISING
BC 337	1	Fast Carry Counter	Eight stage counter with common reset and independent set and count inputs which can be connected to provide an eight bit binary count or a two stage BCD count. The independent set inputs allow a starting count to be preset.
FA 335	1	Gated Flip-Flop	Four independent Flip-Flops.
PA 336	1	Power Amplifier	Six three input NAND gate power drivers.
DI 335	2	Multi-input NAND Gate	Eight two input NANDS. Two two Input NANDS with separate loads.
CC 055	3	Solenoid Driver	Four independent solenoid drivers.

SECTION 2

INSTALLATION

PHYSICAL DESCRIPTION

The PTRPC option, contained in a 1 x 3μ-BLOC, can be mounted in any vacant BLOC location within the option drawer of the main frame or in an option bay. The connector and PAC allocations within the BLOC are shown in LBD No. EO83 and the connector pin assignments are given in LBD No. EO81 and EO82.

DEVICE CABLES

Honeywell Paper Tape Reader

Table 2-1 and Figure 2-1 illustrate the Paper Tape Reader plug connections and device cable respectively.

The device cable, made to the customer's requirements within the maximum length of 50 ft., is fitted at one end with a Painton connector which plugs into the Paper Tape Reader. The other end of the cable is fitted with a Honeywell card connector which plugs into the PTRPC.

Slow Speed Paper Tape Punch

The Slow Speed Paper Tape Punch device cable and plug connections are shown in Figure 2-2 and Table 2-2 respectively.

The device cable, made to the customer's requirements within the maximum permissable length of 50 ft., is fitted at one end with a Cannon connector which plugs into the Paper Tape Punch Unit. The other end of the cable is fitted with a Honeywell card connector which plugs into the PTRPC.

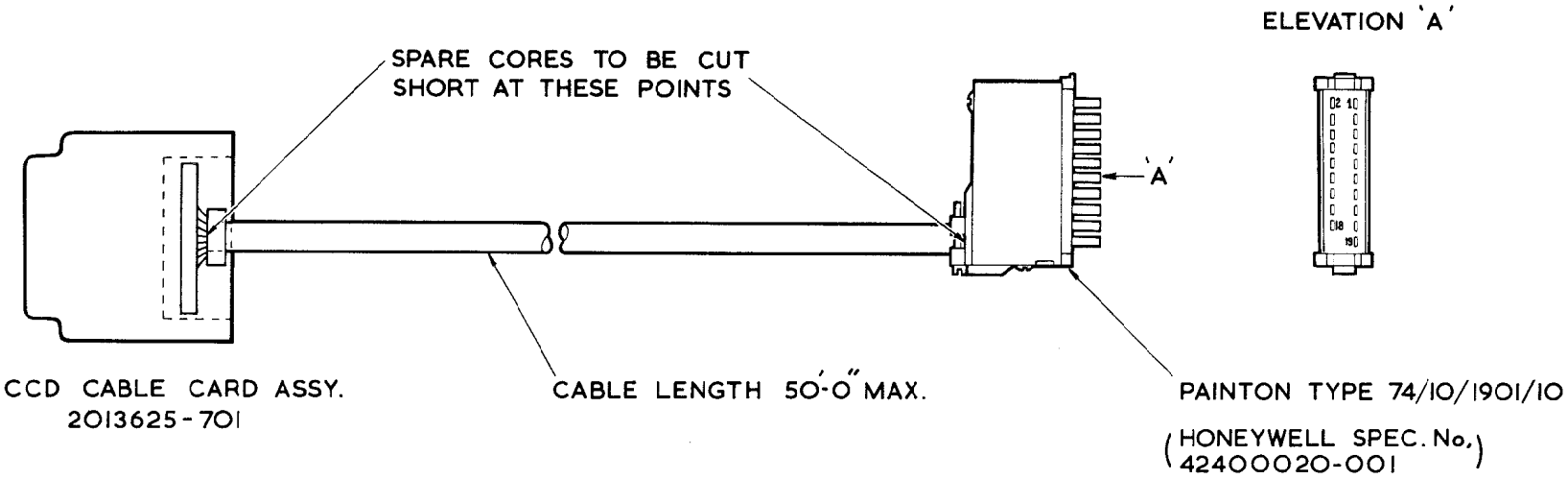
High Speed Paper Tape Punch

The device cable from the PTRPC is connected to the High Speed Facit Punch Unit through the Honeywell Electronic Control Unit (the Electronic Control Unit to Punch Unit cable, 8 ft. long, is a standard Facit item). The device cable from the PTRPC to the Electronic Control Unit is made to the customer's requirements within the maximum permissable length of 50 ft. An illustration of the device cable is shown in Figure 2-3 with the plug connections given in Table 2-3.

TABLE 2-1

READER UNIT TO INTERFACE MODULE

READER UNIT	50 ft. Max.	INTERFACE MODULE
Painton Connector		Card Connector
FJ02 01	GROUND	C17 31
02	RCH01	01
03	RSTRT	12
04	RCH02	02
06	RCH03	03
08	RCH04	04
10	RCH05	05
11	RSTOP	14
12	RCH06	06
13	ONLIN	15
14	RCH07	07
16	RCH08	08
18	SPRK1	13
19	SPRK2	11



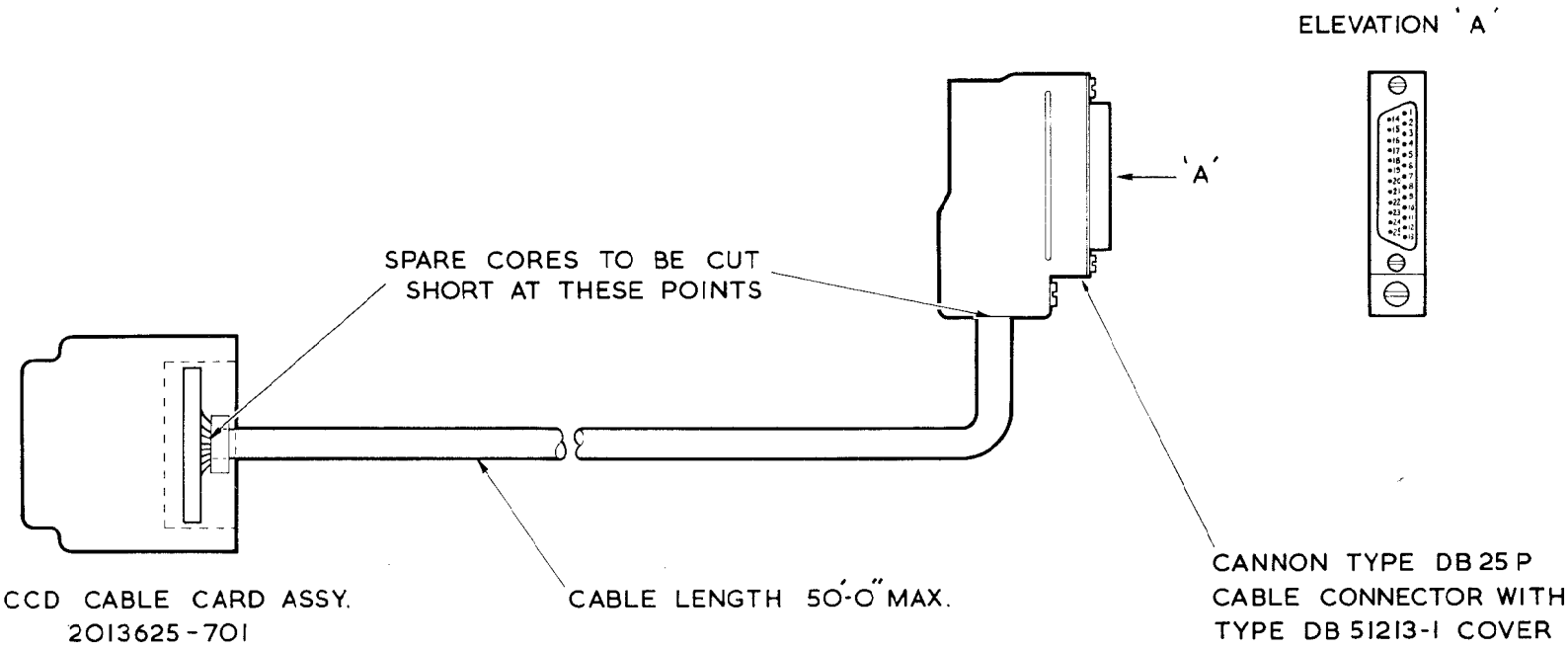
NOTES :
1. ALL SPARE TWISTED PAIRS TO BE CUT SHORT AS INDICATED ON DWG.
2. REFER TO K DOC. 42510392 FOR CONNECTIONS.
3. ALL BLACK WIRES ARE EARTHED AT EARTH PLATE PIN 33 ON CCD CABLE CARD.

Figure 2-1 Reader Interface Cable Assembly

TABLE 2-2

SLOW SPEED PUNCH UNIT TO INTERFACE MODULE

PUNCH UNIT		50 ft. Max.	INTERFACE MODULE	
Cannon Connector			Card Connector	
P1	06	INFC6+	A17	01
	12	PRDYS+		05
	03	INFC3+		06
	04	INFC4+		12
	11	START+		13
	08	INFC8+		17
	05	INFC5+		18
	24	PNCH6+		25
	01	INFC1+		24
	10	PCHSD-		27
	07	INFC7+		29
	02	INFC2+		30
	25	EARTH		31



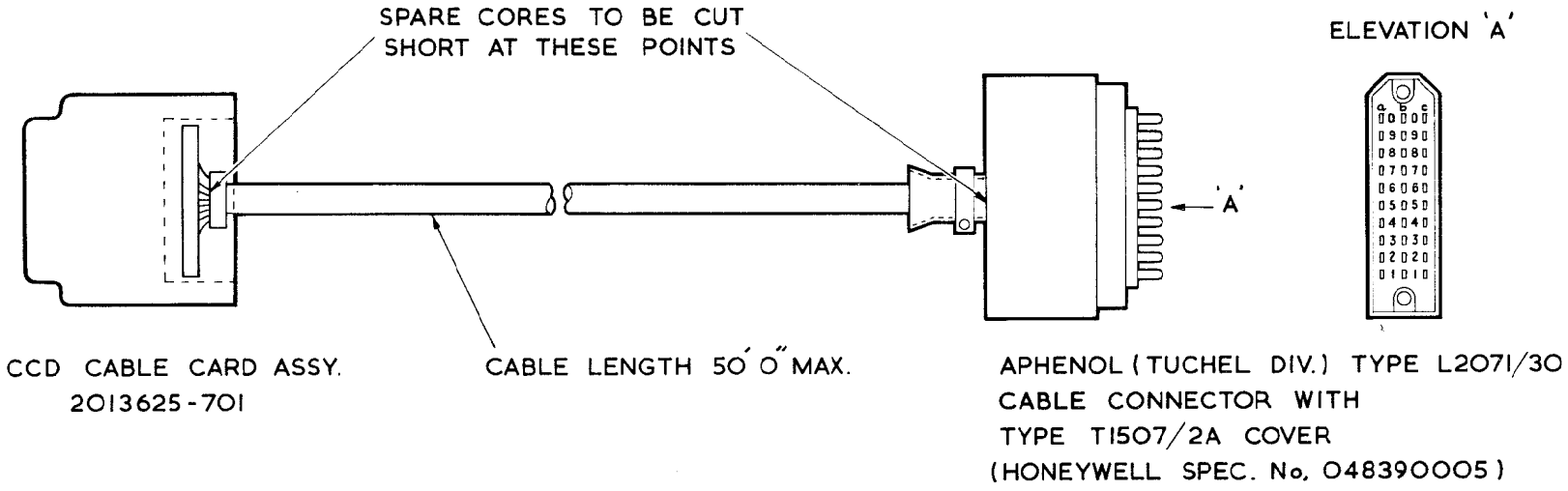
NOTES :
1. ALL SPARE TWISTED PAIRS TO BE CUT SHORT AS INDICATED ON DWG.
2. REFER TO K DOC. 42510393 FOR CONNECTIONS.
3. ALL BLACK WIRES ARE EARTHED AT EARTH PLATE PIN 33 ON CCD CABLE CARD.

Figure 2-2 Slow Speed Punch Interface Cable Assembly

TABLE 2-3

ELECTRONIC UNIT TO INTERFACE MODULE

ELECTRONIC UNIT			50 ft. Max.	INTERFACE MODULE	
Tuchel Connector				Card Connector	
PO1	a	1	PWENB+	A 11	3
		2	TPOUT-		28
		3	EARTH		31
		4	GPRDY+		15
		5	FDDVR+		21
		6	DTD01+		23
		7	DTD02+		20
		8	DTD01-		25
		9	RLDVR+		26
		0	BTAPE-		27
	b	1	DTD07-		7
		2	DTD08+		2
		3	VOLT 6V+		30
		4	OSCOP-		24
		5	BRDVR+		18
		6	OSCIP-		12
		7	STPXX+		6
		8	MCOMB-		1
		9	DTD05-		13
		0	STRXX+		9
	c	1	DTD07+		5
		2	DTD08-		4
		3	DTD06+		8
		4	DTD06-		10
		5	DTD05+		11
		6	DTD02-		22
		7	DTD04+		14
		8	DTD04-		16
		9	DTD03+		17
		0	DTD03-		19



NOTES :
1. ALL SPARE TWISTED PAIRS TO BE CUT SHORT AS INDICATED ON DWG.
2. REFER TO K DOC. 42510240 FOR CONNECTIONS.
3. ALL BLACK WIRES ARE EARTHED AT EARTH PLATE PIN 33 ON CCD CABLE CARD.

Figure 2-3 Electronic Control Unit Interface Cable Assembly(High Speed Punch)

SECTION 3

PROGRAMMING

INSTRUCTION FORMAT

General information on programming is given in the following reference manuals:

Programmers Reference Manual Doc. No. 130071585 (DDP-516)

Programmers Reference Manual Doc. No. 130071628 (DDP-416)

Programmers Reference Manual Doc. No. 42400343401A(H316 and DDP-516)

Programmed instructions are transferred from the computer to the PTRPC via the standard I/O bus and address lines. The instruction format is shown in Figure 3-1.

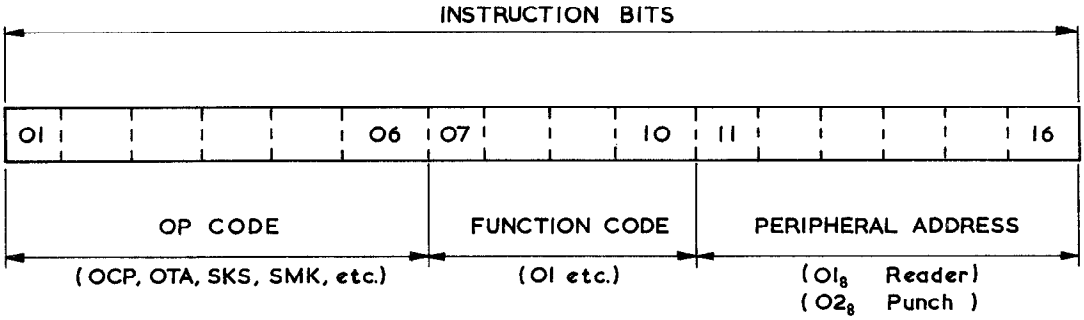


Figure 3-1 Instruction Format

The OP code and function code are translated by the reader interface logic into instructions for the reader. The interface logic, shown in the logic block diagrams at the end of the text, is described in detail in Section 4.

INSTRUCTION COMPLEMENT

The instruction complement summary is listed in Table 3-1.

TABLE 3-1

INSTRUCTION COMPLEMENT SUMMARY

INSTRUCTION	DEFINITION
Reader Control	
OCP 0001	Start tape motion.
OCP 0101	Stop tape motion.
Reader Checks	
SKS 0001	Skip if reader ready.
SKS 0401	Skip if reader not interrupting.
Input Instructions	
INA 0001	Transfer data to 'A' register.
INA 0101	Clear 'A' register and transfer data.
Set Mask Instruction	
SMK 0020	Set interrupt mask Flip-Flop.(Reader; bit 9 on output bus. Punch; bit 10 on output bus).
Output Instruction	
OTA 0002	Transfer data from the 'A' register.
Punch Checks	
SKS 0002	Skip if punch ready.
SKS 0102	Skip if punch power on.
SKS 0402	Skip if punch not interrupting.

OCP Instructions (Reader Control)

Provided the reader power is on, an OCP 0001 instruction initiates continuous reading. A further OCP instruction (OCP 0101) is required to stop the reader after the last frame is read.

OCP 0001	Start reader tape motion
OCP 0101	Stop reader tape motion

SKS Instructions

SKS instructions are used to test the status of the reader or punch. The SKS sends out its device and function code on the I/O bus and then looks for a status signal on DRLIN. If an affirmative status signal (DRLIN-low) is received, within the prescribed time interval, the next instruction is skipped. If an affirmative status signal is not received the next instruction is effected.

SKS 0001: Skip the next instruction if the reader is in a ready state. The reader is ready when a character is available in the reader buffer.

SKS 0002: Skip the next instruction if the punch is in a ready state. The punch is ready when it has completed punching the previous character, and the punch buffer is ready to accept another character.

SKS 0102: Skip the next instruction if the punch power is on.

SKS 0401: Skip the next instruction if the reader is not interrupting. The reader is interrupting when a character is available for input and the reader mask flip-flop is set.

SKS 0402: Skip the next instruction if the punch is not interrupting. The punch is interrupting when the punch mask flip-flop is set and the punch buffer is ready to accept a character.

INA Instructions

The INA instruction inputs data from the device into the 'A' register via the input bus (INB).

The device code and function code of the INA instruction are sent out on the I/O bus and a ready signal looked for on DRLIN. If a ready signal is received, within a predetermined time interval, the contents of the INB are logically OR'ed with the contents of the 'A' register, the next instruction is skipped, and a reset ready signal is sent out on the RRLIN informing the device that the data has been accepted by the computer. If a ready signal is not received no data transfer takes place and the next instruction is executed.

INA 0001: If a ready signal is received it will cause the information contained in the tape frame to be OR'ed with the eight least significant digits of the 'A' register (tape channel 1 corresponds to register bit 16) and the next instruction to be skipped. If a ready signal is not received the next instruction is executed.

INA 1001: Clears the 'A' register before input occurs otherwise the instruction is the same as INA 0001.

SMK 0020 Instruction

The SMK 0020 instruction sets the standard interrupt mask flip-flop. Each bit of the 'A' register controls the set mask of a specific device (the reader is allocated bit 09 and the punch bit 10). A logical '1' sets the mask and a logical '0' resets it. When the mask is set interrupts can take place.

OTA 0002 Instruction

Execution of this instruction results in an output transfer if the punch ready status is true. The eight least significant bits of the 'A' register are transferred to the device buffer, a punch cycle is initiated and the next instruction is skipped. During a punch cycle the interface responds to this instruction as not ready. If the ready status is not true data output transfer does not take place and the next instruction is executed.

SECTION 4

THEORY OF OPERATION

GENERAL

The signal locations, and signal mnemonics referred to in the following text are described in the Function Index (Table 4-1).

FUNCTIONAL THEORY

Reader

Start Command (OCP 0001)- (LBD No.EO77): The coincidence of OCPXX+, ADB10- and RADXX+A drives RNOCP- low, causing RSTOP- to go high. RSTOP- gated with ONLIN+ and INSTR- causes RSTOP+ to go low and RSTRT+ to go high. RSTOP+ and RSTRT+ are subsequently fed to the reader to control the brake and pinch drivers. With a high signal applied to the pinch roller driver (RSTRT+) and a low signal applied to the brake driver (RSTOP+) the pinch roller driver engages and the brake is released.

With the pinch roller engaged and the brake released tape movement commences and SPRK2+ is detected by the reader. Due to the spacing of the sprocket sensors SPRK2+ is detected just before SPRK1+ (SPRK2+ is still high when SPRK1 is detected). Coincidence of SPRK1 and SPRK2 causes STSPR- to go low setting the sprocket flip-flop. When SPRK1 and SPRK2 are both low RSSPR- will go low and reset the sprocket flip-flop. This system of sprocket production is used to prevent transient signals on the leading and trailing edges of the sprocket signals from producing spurious timing signals.

The falling edge of SPRKT- sets the ready flip-flop (RRDYX+ high). The Reader Ready flip-flop also requires SPRK2+ to produce RRDYX+ ensuring that spurious pulses on the trailing edge of SPRK1+ do not cause a double response. SPRKT+ is fed to the reader buffer logic where it gates the eight data channels from the reader into the reader buffer.

(LBD No.EO76): RRDYX+ is gated in the reader status logic with ADB08-A and ADB10-A (during SKS 0001 command and during the busy test in a INA 0001/1001 command) to indicate the reader status. The resultant signal DRLINR+ is gated with RADXX+A, driving DRLIN- low.

NOTE

The sequence of events described previously occurs during the initial period of SPRKT+ and normally data in the buffer is input to the Central Processor long before SPRKT+ goes low. However, if for some reason no INA command is issued to the reader by the time that SPRKT+ goes low, tape motion is inhibited (LBD No.EO77): SPRKT- is gated with RRDYX+ and if both signals are high (sprocket not present and RRDYX+ not reset by INA command) INSTR- goes low causing RSTOP+ to go high and RSTRT+ to go low, stopping the tape. An INA command issued to the reader when the tape has stopped will reset RRDYX+. When RRDYX+ goes low INSTR- goes high, RSTOP+ and RSTRT+ will again come under the control of RSTOP-, and tape motion will recommence.

Input Command (INA 0001/1001)-(LBD No.EO76): Initially the INA instruction tests for reader busy, interrogating the condition of RRDYX+ as described previously. If RRDYX+ is low DRLIN- remains high, no data transfer is effected and the next instruction is executed. If RRDYX+ is high DRLIN- goes low during the reader busy test. (LBD No.EO77): RADXX+B gates the data from the reader buffer onto the I/P bus. (LBD No.EO76): The Central Processor continues the INA command, accepting data from the I/P bus and transmitting RRLIN- to the interface. RRLIN- is gated with RADXX+A (which is still high) and RRRAD- goes low. (LBD No.EO77): The falling edge of RRRAD- causes RRDYX+ flip-flop to reset and when RRRAD- ends RRDYX- gated with RRRAD- drives CLEAR- low. CLEAR- breaks the recirculation on the reader buffer and the buffer is reset. The controller is then able to accept another character from the moving tape, and the preceding actions (summarised below) are repeated:-

1. Recognise sprocket.
2. Strobe character into buffer and Set Ready.
3. Drive DRLIN-low during busy test in INA command and strobe the data onto the I/P bus.
4. Receive RRLIN- pulse.
5. Reset Ready.
6. Clear buffer.
7. Wait for next sprocket.

Stop Command (OCP 0101) -(LBD No.EO77): The coincidence of OCPXX+, RADXX+A and ABD10+ causes STOCP- to go low resetting RSTOP-. RSTOP+ goes high, RSTRT+ goes low and tape motion ceases.

Interrupt

(LBD No.EO76) : Standard interrupt is controlled by the reader mask flip-flop and the punch mask flip-flop. Coincidence of SMK01+ and OTB09+ sets the reader mask flip-flop, with coincidence of SMK01+ and OTB10 setting the punch mask flip-flop.

If the reader mask flip-flop is set, the reader ready flip-flop drives PIL00- low indicating to the Central Processor that an interrupt is taking place. If the computer performs an SKS0401 command DRLIN- is not driven low, since RINTX- is low, indicating that the reader is interrupting. Similarly, if the punch mask flip-flop is set the punch ready flip-flop causes PIL00- to go to ground and a SKS0402 command will indicate that the punch is interrupting, since PINTX- will be low.

SKS Commands

The status of the reader or punch may be checked by use of the SKS commands shown below :-

SKS0001 Drive DRLIN- line low if reader not busy.

SKS0002 Drive DRLIN- line low if punch not busy.

SKS0102 Drive DRLIN- line low if punch power is on.

SKS0401 Drive DRLIN- line low if reader not interrupting.

SKS0402 Drive DRLIN- line low if punch not interrupting.

Subsequent to each SKS command the command following the SKS is skipped if the DRLIN- line is driven low.

Output Command (OTA0002)

Slow Speed Punch - When the OTA 0002 command is issued the ready state of the interface is confirmed and the character to be punched is placed on the O/P bus.

(LBD No.EO76) : The control pulse RRLIN- is fed to the interface module where it is inverted to drive RRLIN+ high. RRLIN+ gated with PADXX+ drives RRPAD- low and RRPAD+ high. (LBD No.EO78): RRPAD- sets PSTRT+, CLBUF+ goes low, and CLBUF- goes high maintaining recirculation in the common punch buffer. (LBD No.EO79): RRPAD+ gates the character from the O/P bus into the common punch buffer.

(LBD No.EO78): PSTRT- low drives START+ high and the punch cycle commences. (LBD No.EO76):PSTRT- low also prevents the status logic from indicating not busy. (LBD No.EO78): When the punch has accepted the character stored in the buffer PRDYS+ goes low, PSTRT+ is reset, CLBUF+ goes high and START+ goes low. (LBD No.EO76): In the status logic PRDYS+ low takes over from PSTRT- to indicate punch busy, until the punching is complete when PRDYS+ goes high indicating that the next punch instruction may be effected.

High Speed Punch - The following signals received from the punch assist in the control of tape motion :-

STRXX+ indicates that the punch tape motion may commence

STPXX+ indicates that the punch tape motion should cease

GPRDY+ indicates that punching is complete

The execution of an OTA0002 command to the high speed punch is basically similar to that of the slow speed punch, except for variations in the timing and gating requirements. A brief description of the OTA0002 command for the high speed punch is explained in the following paragraphs.

(LBD No.EO80): RRPAD- low sets PRDYF- while RRPAD+ high gates the O/P bus into the common punch buffer. PRDYF+ low sets SIGMO+ which starts the punch motor via RLDVR+ and RLDVR-. During the initial increase in motor speed STRXX+ is transmitted from the punch to the controller (during each revolution of the motor) and gated with SIGMO+ to provide a count for the run-up delay counter. After 256 counts RUDLY+ goes high.

(LBD No.EO78):PRDYF-, RUDLY+ and the next STRXX+A drive FEDAL- low. FEDAL- low sets BRDVR- high causing FDDVR- to go low, thereby initiating tape motion. FDDVR- low sets APCHR+ and causes GTCHR+ to go high gating the common buffer into the high speed punch gating logic. Since GTHOL- is high at this time the data is transferred to the punch. The falling rear edge of STPXX+A resets BRDVR-. FDDVR- goes high and tape motion ceases. When the tape is stationary the punch punches the character prior to GPRDY+A resetting APCHR+. APCHR- high drives GTCHR+ low.

(LBD No.EO80): APCHR+ low resets PRDYF-. PRDYF- going low causes CLBUF- to go low thereby clearing the common buffer.

(LBD No.EO76): PFRDY- indicates to the status logic that the punch is ready for a further OTA command.

Oscillator

A free running oscillator in the High Speed Control Unit starts to oscillate when the punch commands to the High Speed Punch cease. The frequency of the oscillator is set to 0.2 Hz i.e. one cycle occurring every five seconds.

(LBD No.EO80): During a punch command,initiated under program control or manual control, PRDYF+ goes low driving OSCIP- high. OSCIP- initialises the oscillator, preventing the oscillator completing a cycle unless a 5 second delay occurs in the output commands to the punch. If the oscillator is permitted to complete a cycle OSCOP- is transmitted to the controller to reset the SIGMO+ flip-flop, causing the high speed punch motor to stop.

Toggle Switch

The following cycle of events occur in the controller when the toggle switch on the high speed punch is positioned to 'Blank Tape'.

(LBD No.EO80): BTAPE- goes low and BTAPE+ goes high. If the punch is executing a punch cycle at this time PRDYF+ will be low and nothing further will occur until the end of the punch cycle when PRDYF+ goes high. With BTAPE+ high and PRDYF+ high BTAPE-A is driven low and MANSW+ goes high. MANSW+ and PRDYF+ drive MANSW- low, setting PRDYF- flip-flop and driving PFRDY- high to provide a busy indication in the status logic. PRDYF+ low sets SIGMO+ and provides a low input to the PFRDY- gate to continue the busy indication since PRDYF+ low enables MANSW- to go high. PFRDY+ low enables OSCIP- to go high,initialising the 5 second time out oscillator. If the motor is stopped when SIGMO+ goes high STRXX+ provides inputs to the RUDLY+ counter.

(LBD No.EO78): When RUDLY+ goes high the next STRXX+, gated with RUDLY+ and PRDYF-, drives FEDAL- low. The falling edge of FEDAL- sets BRVDR- high, FDDVR- goes low and tape motion commences. The falling edge of FDDVR- sets APCHR+, APCHR+ going high and APCHR- going low, setting GTCHR+ high. Because MANSW- going low has already caused CLBUF- to go low (clearing the common punch buffer) nothing can be gated into the high speed gating logic when GTCHR+ is set high. Tape motion continues until the punch transmits STPXX+ which resets BRDVR- causing the tape motion to cease. When the punch has completed punching the blanks (sprocket hole only) GPRDY+ is transmitted to reset APCHR+.

(LBD No.EO80): APCHR+ low resets PRDYF- If the punch toggle switch is still in the 'Blank Tape' position PRDYF+ gated with MANSW+ drives MANSW- low, setting PRDYF- again, and the preceding cycle of events is repeated until the toggle switch is released.

If the toggle switch is positioned to 'Mark Combination' the preceding cycle of events is applicable with the exception of the following differences :-

1. (LBD No. EO80): MCOMB-A instead of BTAPE-A causes MANSW+ to go high.
2. MCOMB-A sets the HOLES+ flip-flop.
3. HOLES+ gated with APCHR+ drives GTHOL- low.
4. GTHOL- low enables CHAN 1-8+ to go high and all holes are punched.

TABLE 4-1

FUNCTION INDEX

MNEMONIC	DESCRIPTION	LBD/ZONE
ADB08/16-	Address bus: Carries peripheral address and function codes from the Central Processor to the control unit.	LBD No. EO76
APCHR+	Allow Punch Character: Set when Forward Drive signal is sent to High Speed Punch; reset when punching is complete.	LBD No. EO78(D9) and EO80(3E, 4D, 6C).
BFOP 1/8+	Buffer Output: Output from common punch buffer to High Speed gating.	LBD No. EO78 and EO79.
BRDVR+	Brake Driver: Brake signal to High Speed Punch.	LBD No. EO80(4H).
BTAPE-	Blank Tape: Indicates that the High Speed Punch has been manually set to punch blank tape.	LBD No. EO80(1A).
CHAN 1/8+	Channel 1 to 8: Output from High Speed gating to punch solenoid drivers.	LBD No. EO78 and EO80.
CLBUF-	Clear Buffer: Clears the common punch buffer when punching is complete.	LBD No. EO78(16B) and EO80.
CLEAR-	Clear: Clears the reader buffer when an INA command is completed.	LBD No. EO77.
CLMSK-	Clear Mask: Resets the mask Flip-Flop. Derived from CMKXX- or MSTCL-.	LBD No. EO76(5H, 5K)
CLRDY-	Clear Ready: Resets the reader ready Flip-Flop during INA, Master Clear or if the reader is not available.	LBD No. EO77(5K,8A).
CMKXX-	Clear Mask: Clears the masks ready for a new mask setting at the beginning of the SMK command.	LBD No. EO76(2H)

TABLE 4-1

FUNCTION INDEX(Contd.)

MNEMONIC	DESCRIPTION	LBD/ZONE
DACH 1/8-	Data Channels 1 to 8: Information from the reader gated with the sprocket. It is used to set the buffer at sprocket time.	LBD No. EO77
DRLIN-	Device Ready Line: Used during the status check to indicate the condition of the peripheral.	LBD No. EO76(17C)
DRLNP+	Device Ready Line Punch: Indicates the condition of the punch to DRLIN-	LBD No. EO76(15C)
DRLNR+	Device Ready Line Reader: Indicates the condition of the reader to DRLIN-	LBD No. EO76(14H)
DTD 01/08±	Data Drivers 1 to 8: Drive the punch solenoids.	LBD No. EO80
FDDVR+	Feed Driver: Causes tape motion in the High Speed Punch.	LBD No. EO80(4J)
FEDAL-	Feed Allow: Sets BRDVR- to enable tape motion.	LBD No. EO78(4B)
GPRDY+	'G' Ready Pulse: High Speed Punch timing signal indicating that punching is complete and that the punch is ready to accept the next OTA command.	LBD No. EO80(8J)
GTCHR+	Gate Character: Gates the output of the common punch buffer into the high speed gating logic.	LBD No. EO78
GTHOL-	Gate Holes: Enabled by the manual switch on the High Speed Punch. Gates all holes into the High Speed Punch gating logic.	LBD No. EO78 and EO80(5D).
HOLES+	Holes: Indicates that the High Speed Punch toggle switch is in the 'Mark Combination' position.	LBD No. EO80(4D)
INB 09/16-	Input Bus 9 to 16: Transfers reader data from the controller to the Central Processor (Reader Bit 1=INB16, Read Bit 8=INB09).	LBD No. EO77
INFC 1/8-	Information Channels 1 to 8: Output from the common punch buffer to the Slow Speed Punch solenoids.	LBD No. EO79

TABLE 4-1

FUNCTION INDEX (Contd.)

MNEMONIC	DESCRIPTION	LBD/ZONE
INRDY+	Inhibit Ready: Derived from OSCOP- or TPOUT-; applicable to the High Speed Punch.	LBD No. EO80(4A)
INSTR-	Inhibit Start: Inhibits reader tape motion if the sprocket pulse has ended and no INA command has yet been given.	LBD No. EO77(6C)
MANSW-	Manual Switch: Indicates whether or not the toggle switch on the High Speed Punch has been operated.	LBD No. EO78(13B) and EO80(5B).
MCOMB-	Mark Combination: Indicates that the toggle switch on the High Speed Punch is set to punch all holes.	LBD No. EO80(1B).
MSTCL-	Master Clear: Resets Masks, APCHR, PSTRT, SIGMO, HOLES, RRDYX, I/P Buffer, O/P Buffer. Sets BRDVR, RSTOP, PRDYF.	LBD No. EO76(1H) EO77(5B,1K) EO78(4C, 6D,11C), EO80(5D,3F,7D)
OCPLS-	Output Control Pulse: Initiates any action required by an OCP command.	LBD No. EO77(1B).
ONLIN+	On Line: Indicates that the reader is powered up and in the Start Mode.	LBD No. EO77(1A)
OSCIP-	Oscillator Inhibit Pulse: Initialises the oscillator in the High Speed Punch Electronic Control Unit.	LBD No. EO80(9B)
OSCOP-	Oscillator Output Pulse: Used to reset SIGMO+ if there is no output to the High Speed Punch for 5 seconds.	LBD No. EO80(3A, 3F)
OSCRS-	Oscillator Reset: Resets SIGMO+ Flip-Flop at OSCOP-time.	LBD No. EO80(5G)
OTB09/16-	Output Bus 9 to 16: Carries output data and mask code from the Central Processor to the PTRPC.	LBD No. EO76 and EO79
PADXX+	Punch Addressed: Decoded address of 0002 on the address bus.	LBD No. EO76 (6B, 16C)
PCHSD-	Punch Stepping Direction: (Tied to ground) Enables the Slow Speed Punch to step in the forward direction only.	LBD No. EO81

TABLE 4-1

FUNCTION INDEX (Contd.)

MNEMONIC	DESCRIPTION	LBD/ZONE
PFRDY-	Punch Fast Ready: Indicates the condition of the High Speed Punch to the status logic.	LBD No. EO76(11D) and EO80(8A).
PILOO-	Priority Interrupt Line: Interrupts the Central Processor if the reader mask Flip-Flop is set and the reader is ready, or punch mask set with punch ready.	LBD No. EO76(9H)
PINTX-	Punch Interrupt: Drives PILOO- low if the punch mask Flip-Flop is set and the punch is ready.	LBD No. EO76(7G, 13D)
PMASK+	Punch Mask: Flip-Flop set by SMK command coincident with bit 10 on the O/P bus.	LBD No. EO76(6G)
PRDYF+	Punch Ready Fast: Flip-Flop indicating that punching has been completed by the High Speed Punch.	LBD No. EO80(1B, 6C, 4G)
PRDYS+	Punch Ready Slow: Ready signal from the Slow Speed Punch.	LBD No. EO76(11A) and EO78(11B).
PRDYX+	Punch Ready: Common signal indicating that the particular punch connected is ready.	LBD No. EO76(13B, 6G)
PSTRT+	Punch Start: Starts the Slow Speed Punch and provides recirculation in the common punch buffer.	LBD No. EO78(13B)
PWENB+	Power Enable: Indicates to the status logic that the punch power (Slow Speed Punch or High Speed Punch) is on.	LBD No. EO76(11D)
RADXX-	Reader Addressed: Decoded address of 0001 on the address bus.	LBD No. EO76(5C)
RBUF 1/8+	Reader Buffer 1 to 8: Output of the reader buffer prior to being gated with RADXX+B and placed on the I/P bus lines.	LBD No. EO77
RCH01/08+	Reader Channels 1 to 8: Input to the controller from the sense amplifiers.	LBD No. EO77
RINTX-	Reader Interrupt: Drives PILOO- low if the reader mask Flip-Flop is set and the reader is ready.	LBD No. EO76(7J, 11H)
RLDVR+	Relay Driver: Operates the motor relay in the Electronic Control Unit (High Speed Punch).	LBD No. EO80(9C)

TABLE 4-1

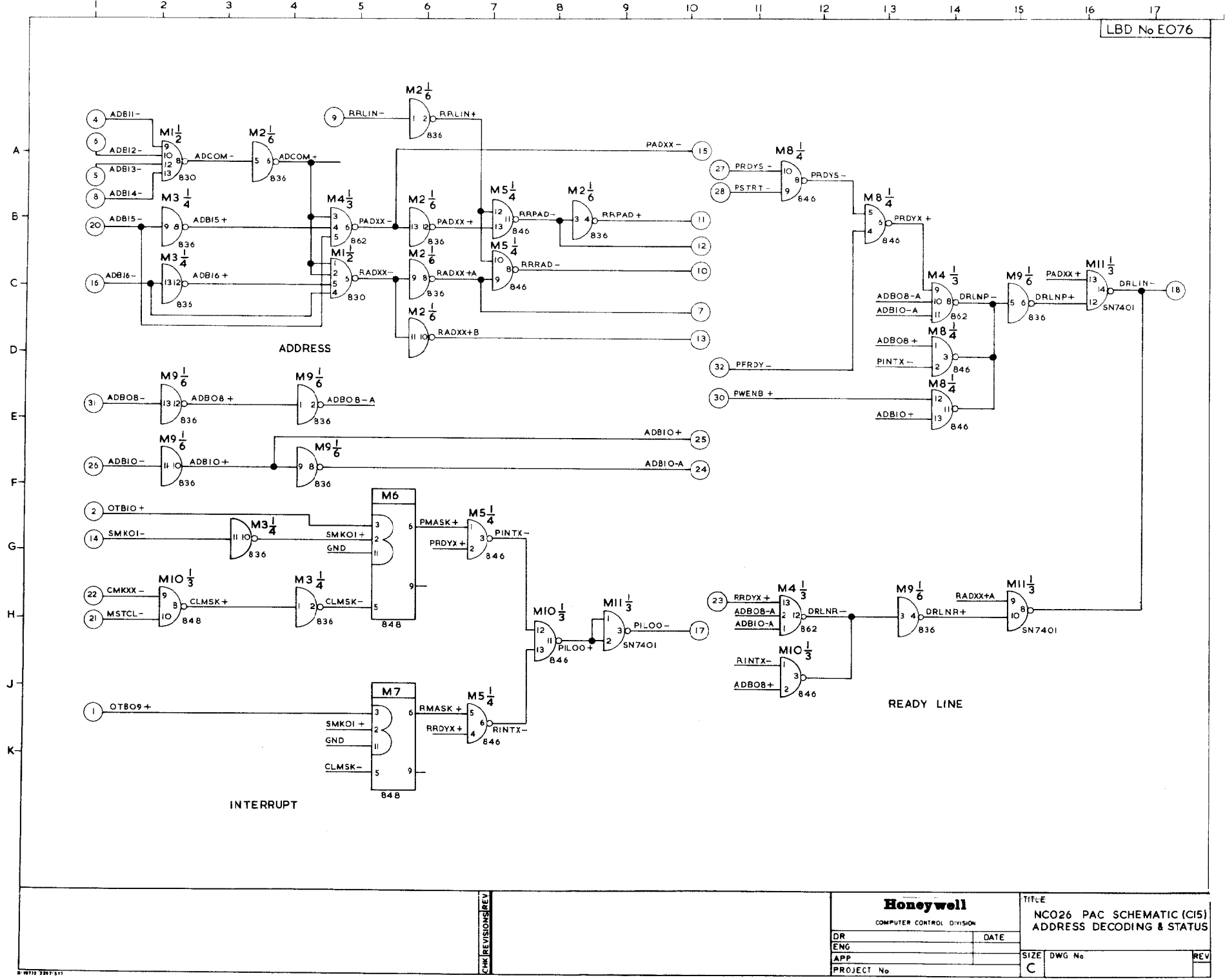
FUNCTION INDEX (Contd.)

MNEMONIC	DESCRIPTION	LBD/ZONE
RMASK+	Reader Mask: Flip-Flop set by SMK command coincident with bit 9 on the output bus.	LBD No. EO77(6J)
RNOCP-	Run Output Control Pulse: Derived from OCP0001 command. Initiates reader tape movement.	LBD No. EO77(5A)
RRDYX+	Reader Ready: Reader has read a character into the buffer and the controller is ready for an INA command.	LBD No. EO76(7K,11H), and EO77(5C, 7J)
RRLIN-	Reset Ready Line: Terminates an INA command or initiates an OTA command.	LBD No. EO76(5A)
RRPAD+	Reset Ready Punch Addressed: Combination of RRLIN and PADXX. Initiates an OTA command to the punch.	LBD No. EO76(9B) and EO79
RRRAD-	Reset Ready Reader Addressed:Combination of RRLIN and RADXX. Terminates an INA command to the reader.	LBD No. EO76(8C) and EO77(1J, 7K)
RSCTR-	Reset Counter: Resets the run-up delay counter.	LBD No. EO80 (9F)
RSSPR-	Reset Sprocket: Derived from SPRK1- and SPRK2-	LBD No. EO77(7G)
RSTOP+	Reader Stop: Activates the reader brake solenoid.	LBD No. EO77(8A)
RSTRT+	Reader Start: Activates the reader pinch solenoid.	LBD No. EO77(8C)
RUDLY+	Run-Up Delay: Output of the run-up delay counter. Inhibits an OTA command to the High Speed Punch until the motor has run-up to a constant speed.	LBD No. EO78(3B) and EO80(12G)
SIGMO+	Signal Motor: Operates the motor relay in the High Speed Punch Electronic Control Unit and initialises the oscillator(via OSCIP).	LBD No. EO80(8C)
SMK01-	Set Mask: Gates the output bus bits onto the Mask Flip-Flops during an SMK command.	LBD No. EO76(1G)

TABLE 4-1

FUNCTION INDEX (Contd.)

MNEMONIC	DESCRIPTION	LBD/ZONE
SPRK1+	Sprocket 1: The reader sprocket signal in line with the data holes.	LBD No. EO77(3E)
SPRK2+	Sprocket 2: The sprocket signal derived from the sprocket hole immediately following the data. Starts slightly earlier than SPRK1 due to the spacing of the sensors.	LBD No. EO77(3E, 5J)
SPRKT+	Sprocket: Information gating pulse derived from SPRK1 and SPRK2.	LBD No. EO77
START+	Start: Initiates the punch cycle in the Slow Speed Punch.	LBD No. EO78(17D)
STBF 1/8-	Store Buffers 1 to 8: Input to common punch buffer subsequent to gating with RRPAD+.	LBD No. EO79
STCTR+	Step Counter: Derived from STRXX+ from the High Speed Punch.	LBD No. EO80(10E)
STOCP-	Stop Output Control Pulse: Stops the reader tape motion. Derived from OCP0101.	LBD No. EO77(5B)
STPXX+	Stop: High Speed Punch timing signal that stops tape motion and enables punching to commence.	LBD No. EO78(3C) and EO80(8H)
STRXX+	Start: High Speed Punch timing signal that enables tape motion to commence.	LBD No. EO78(3B) and EO80(8G)
STSPR-	Set Sprocket: Derived from SPRK1+ and SPRK1+.	LBD No. EO77(7E)
TPOUT-	Tape Out: Warning from the High Speed Punch to indicate that only 5% of the tape remains.	LBD No. EO80(3A)


LBD No EO76
ADDRESS
INTERRUPT
READY LINE
ADBII-
ADBI2-
ADBI3-
ADBI4-
ADBI5-
ADBI6-
ADCOM-
ADCOM+
ADBI5+
ADBI6+
RRLIN-
RRLIN+
PADXX-
PADXX+
RADXX-
RADXX+A
RADXX+B
RRPAD-
RRPAD+
RRRAD-
PRDYS-
PSTRT-
PRDYX+
PFRDY-
PWENB+
ADBO8-
ADBO8+
ADBO8-A
PINTX-
ADBIO-
ADBIO+
ADBIO-A
OTBIO+
SMKOI-
SMKOI+
GND
PMASK+
PRDYX+
PINTX-
CMKXX-
MSTCL-
CLMSK+
CLMSK-
PILOO+
PILOO-
OTBO9+
RMASK+
RRDYX+
RINTX-
RRDYX+
ADBO8+
RINTX-
DRLNP-
DRLNP+
DRLNR-
DRLNR+
RADXX+A
PADXX+
DRLIN-
SN7401
M6
M7
836
830
862
846
848
Honeywell
COMPUTER CONTROL DIVISION
DR
DATE
ENG
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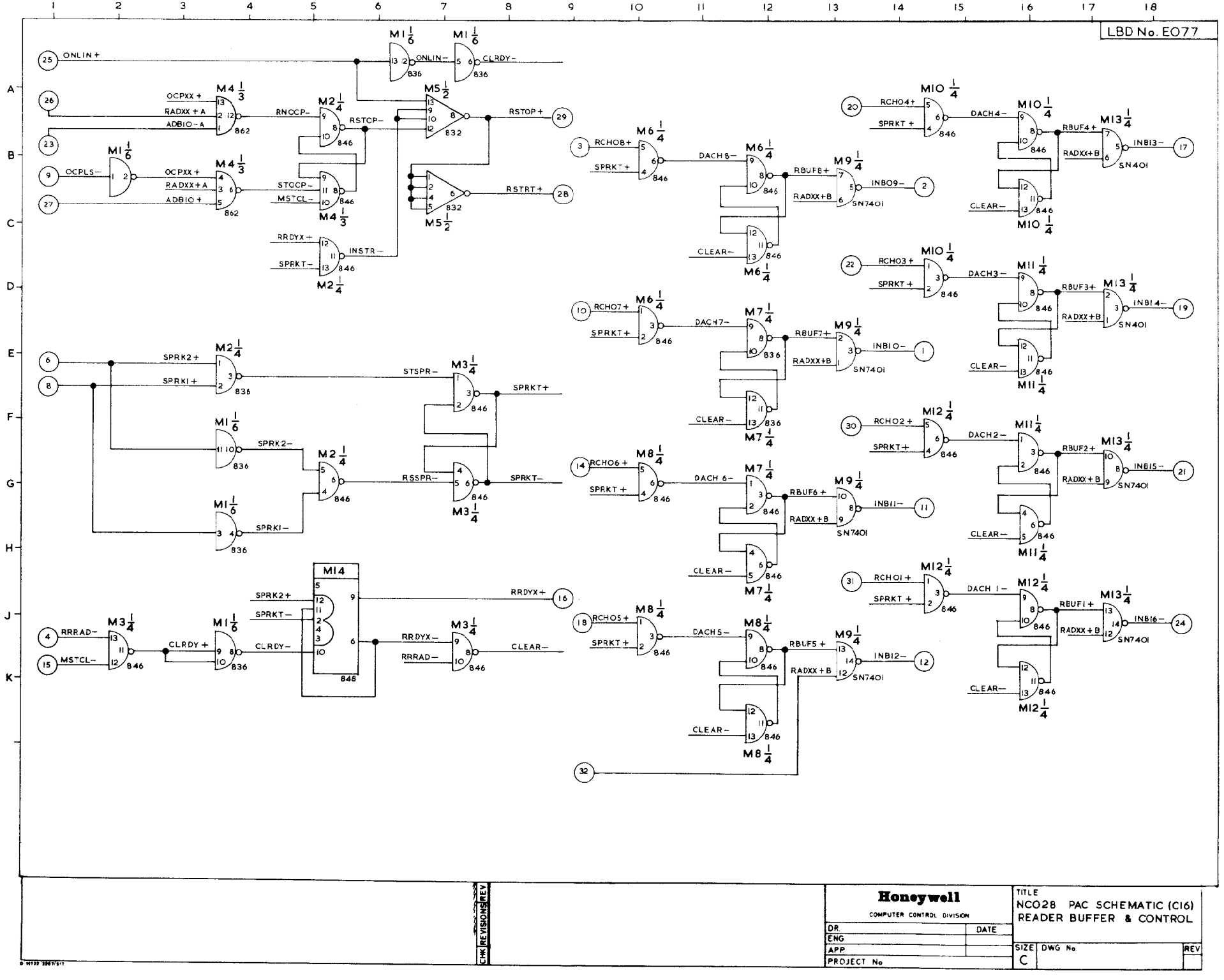
SIZE
C
DWG No
REV
CHK
REVISIONS
REV


LBD No. E077
ONLIN+
OCPXX+
RADXX+A
ADBIO-A
OCPLS-
OCPXX+
RADXX+A
ADBIO+
RNOCP-
RSTOP+
RSTRT+
STOCP-
MSTCL-
RRDYX+
SPRKT-
INSTR-
RCHO8+
SPRKT+
DACH8-
RBUF8+
RADXX+B
INB09-
CLEAR-
RCHO4+
DACH4-
RBUF4+
INB13-
RCHO7+
DACH7-
RBUF7+
INB10-
RCHO3+
DACH3-
RBUF3+
INB14-
SPRK2+
SPRKI+
STSPR-
SPRKT+
SPRK2-
RSSPR-
SPRKI-
RCHO2+
DACH2-
RBUF2+
INB15-
RCHO6+
DACH 6-
RBUF6+
INB11-
RCHO1+
DACH 1-
RBUF1+
INB16-
RRRAD-
MSTCL-
CLRDY+
CLRDY-
RRDYX-
RCHO5+
DACH5-
RBUF5+
INB12-
RADXX+B
CLEAR-
SN7401
836
846
862
832
Honeywell
COMPUTER CONTROL DIVISION
TITLE
NCO28 PAC SCHEMATIC (C16)
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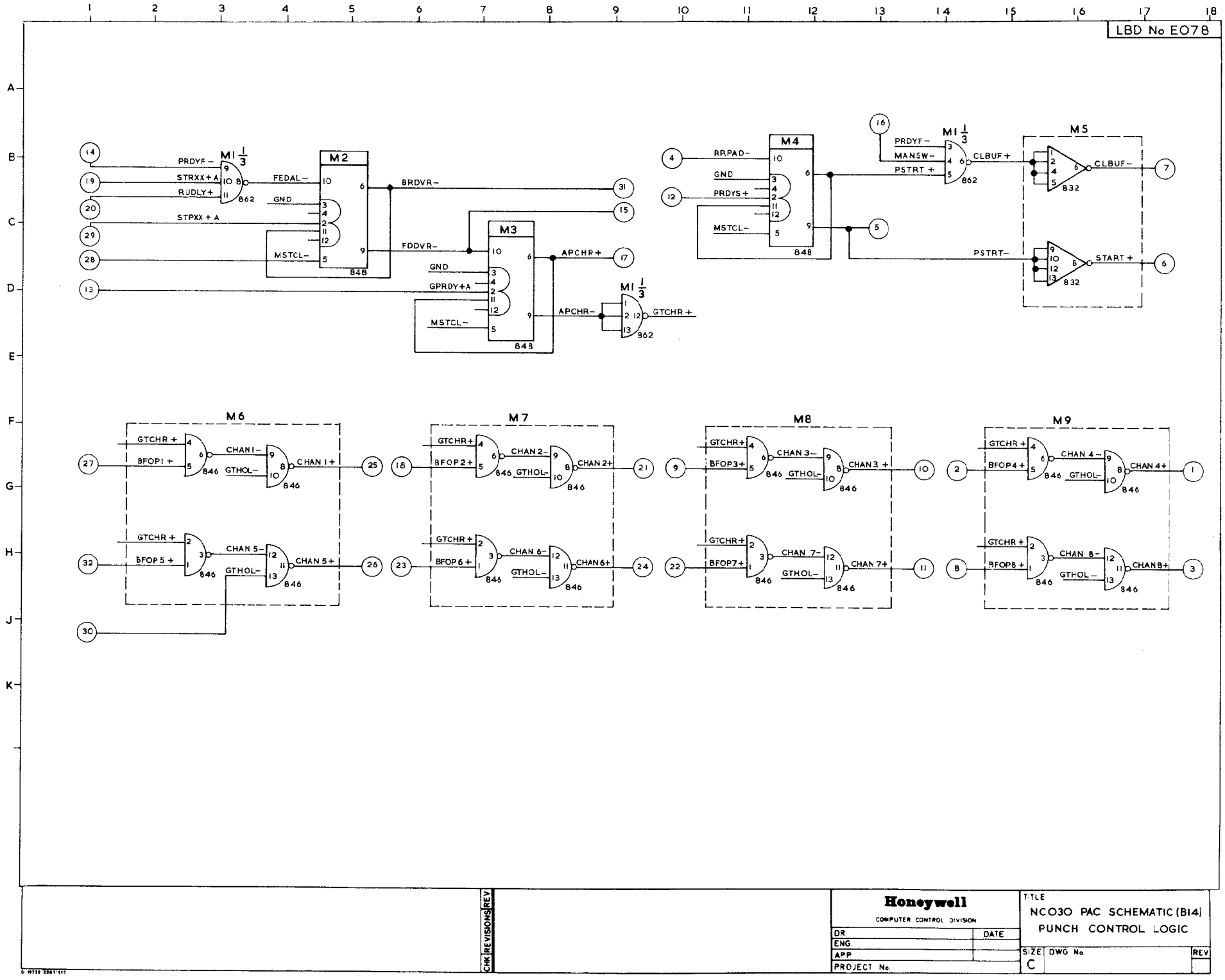
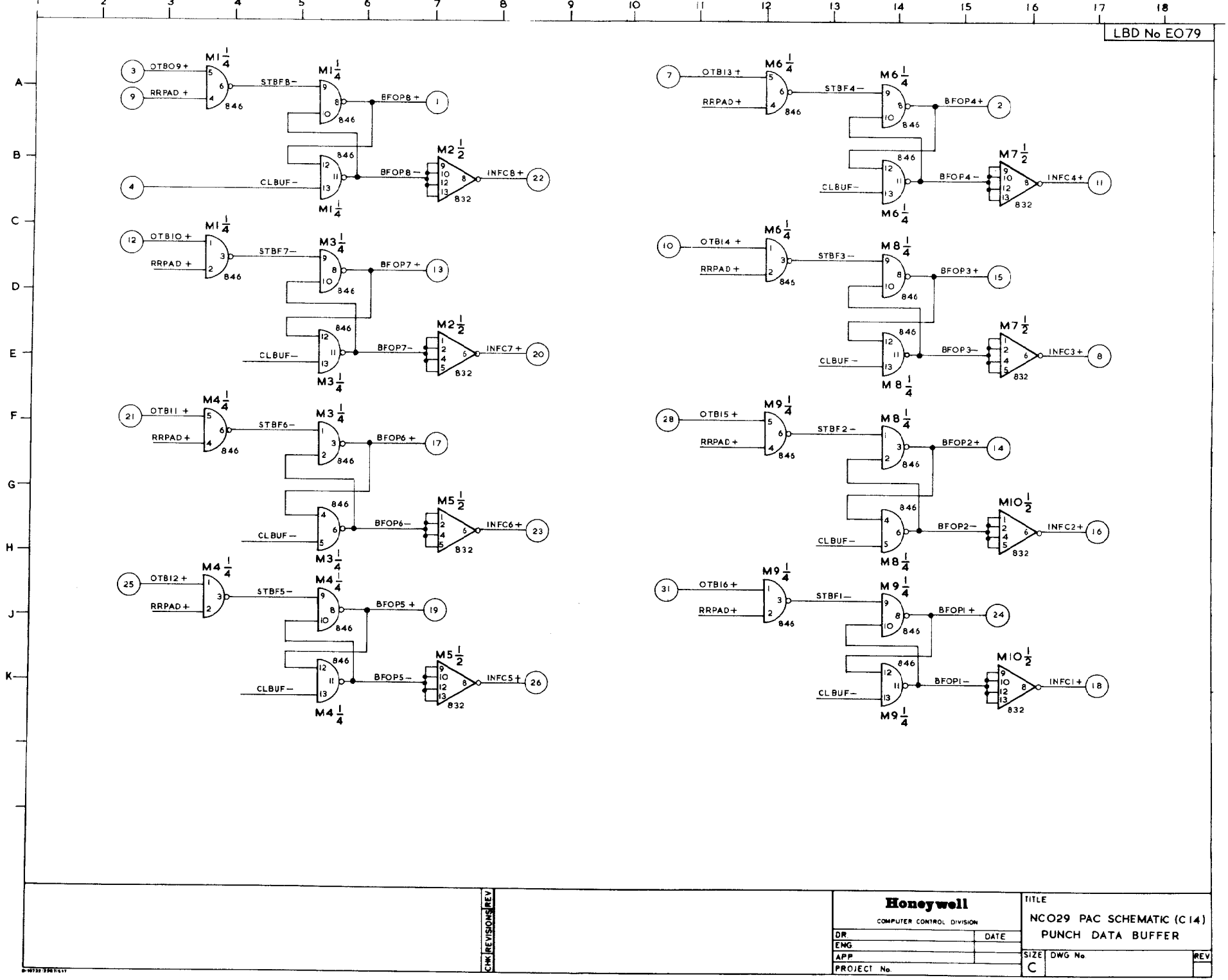
SIZE C
DWG No.
REV
DR
ENG
APP
PROJECT No
DATE
CHK
REVISIONS
REV


LBD No E078
M1 1/3
M2
M3
M4
M5
M6
M7
M8
M9
PRDYF –
STRXX + A
RUDLY +
STPXX + A
FEDAL –
BRDVR –
FDDVR –
GND
MSTCL –
GPRDY + A
APCHR +
APCHR –
GTCHR +
RRPAD –
PRDYS +
MANSW –
PSTRT +
CLBUF +
CLBUF –
PSTRT –
START +
BFOP1 +
CHAN 1 –
CHAN 1 +
GTHOL –
BFOP2 +
CHAN 2 –
CHAN 2 +
BFOP3 +
CHAN 3 –
CHAN 3 +
BFOP4 +
CHAN 4 –
CHAN 4 +
BFOP5 +
CHAN 5 –
CHAN 5 +
BFOP6 +
CHAN 6 –
CHAN 6 +
BFOP7 +
CHAN 7 –
CHAN 7 +
BFOP8 +
CHAN 8 –
CHAN 8 +
Honeywell
COMPUTER CONTROL DIVISION
TITLE
NC030 PAC SCHEMATIC (B14)
PUNCH CONTROL LOGIC
DR
ENG
APP
PROJECT No.
DATE
SIZE C
DWG No.
REV
CHK
REVISIONS
REV


LBD No EO79
OTBO9+
RRPAD+
STBF8-
BFOP8+
CLBUF-
BFOP8-
INFC8+
OTBI0+
STBF7-
BFOP7+
BFOP7-
INFC7+
OTBI1+
STBF6-
BFOP6+
BFOP6-
INFC6+
OTBI2+
STBF5-
BFOP5+
BFOP5-
INFC5+
OTBI3+
STBF4-
BFOP4+
BFOP4-
INFC4+
OTBI4+
STBF3-
BFOP3+
BFOP3-
INFC3+
OTBI5+
STBF2-
BFOP2+
BFOP2-
INFC2+
OTBI6+
STBFI-
BFOPI+
BFOPI-
INFCI+
846
845
832
Honeywell
COMPUTER CONTROL DIVISION
DR
DATE
ENG
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PROJECT No.
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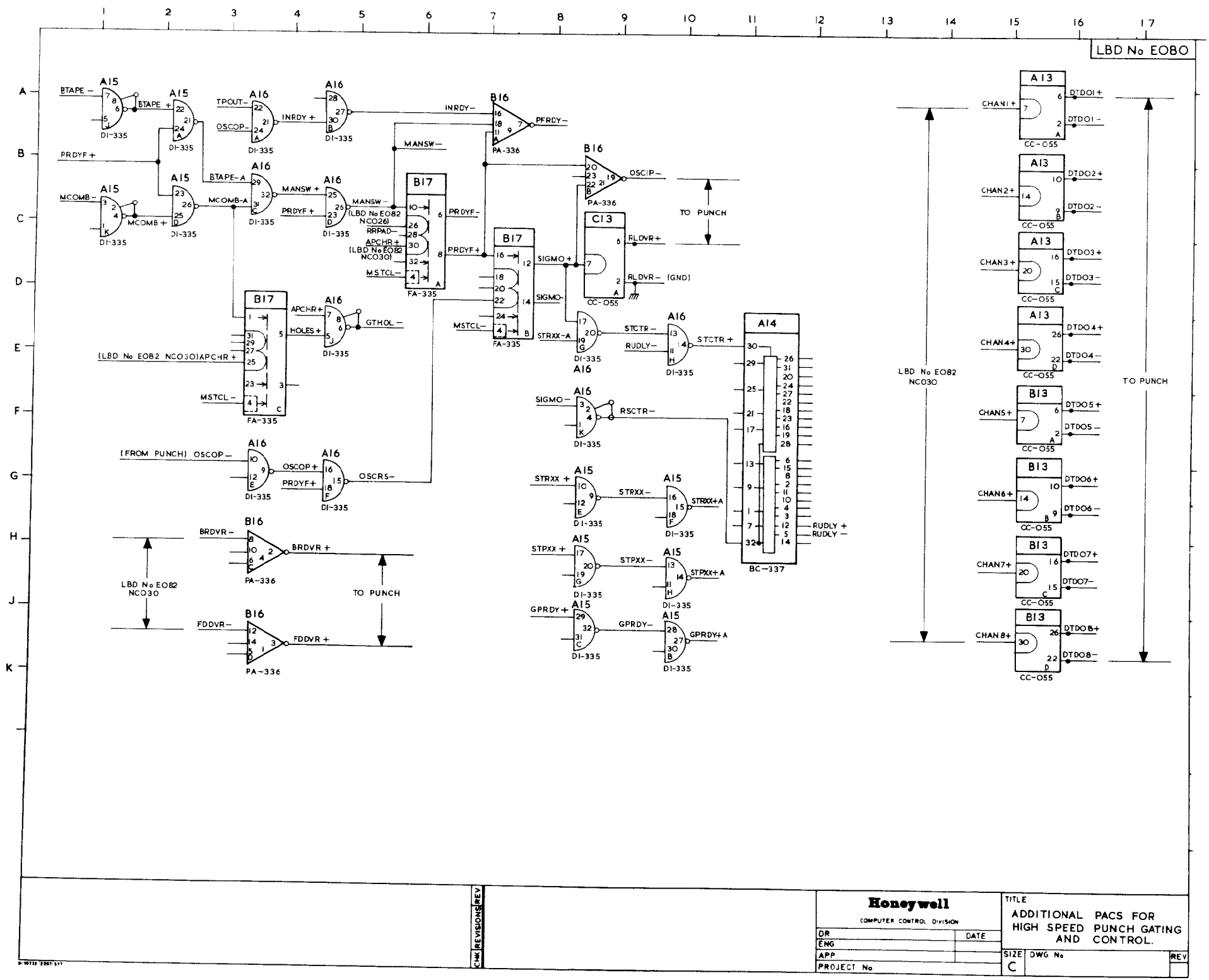
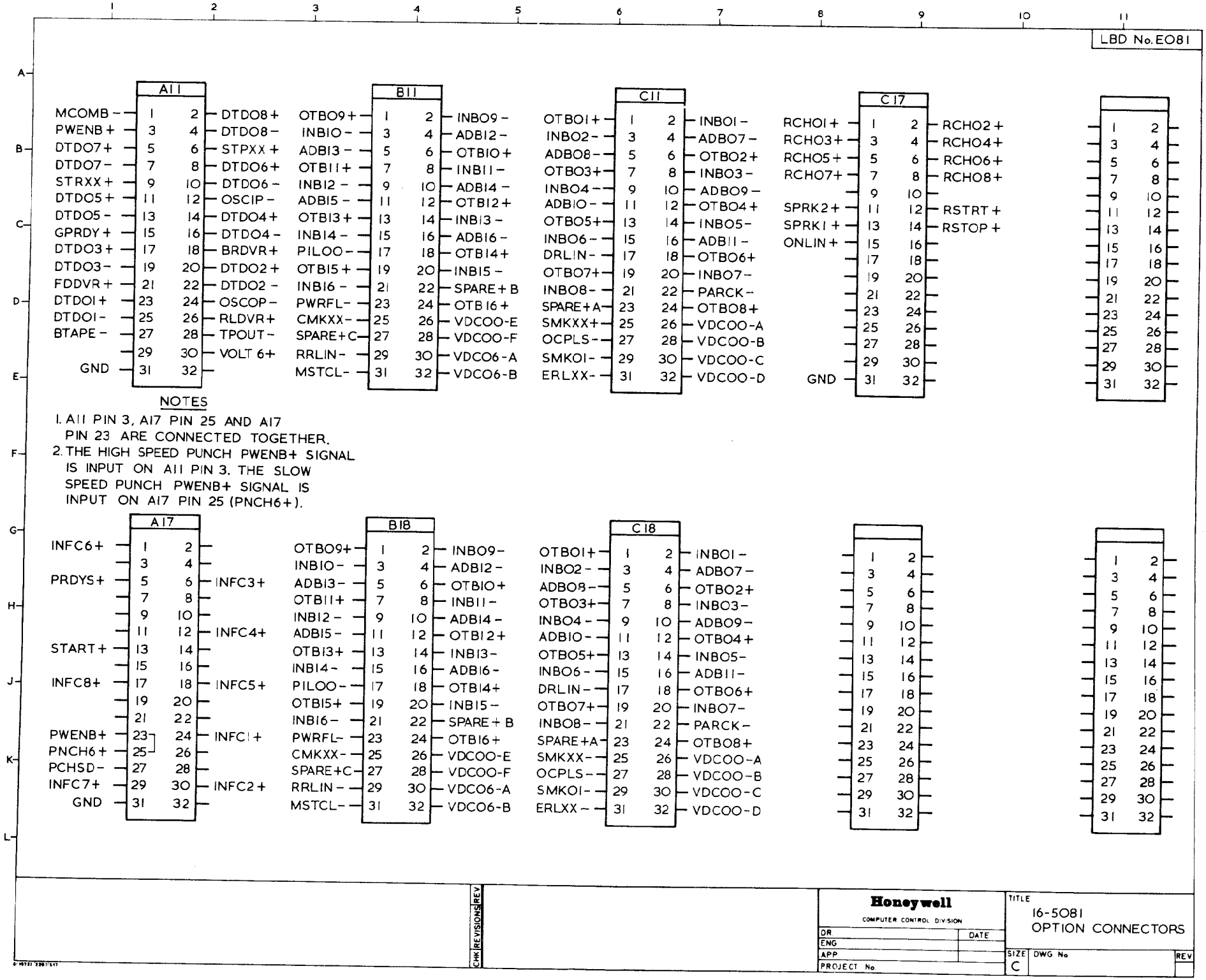
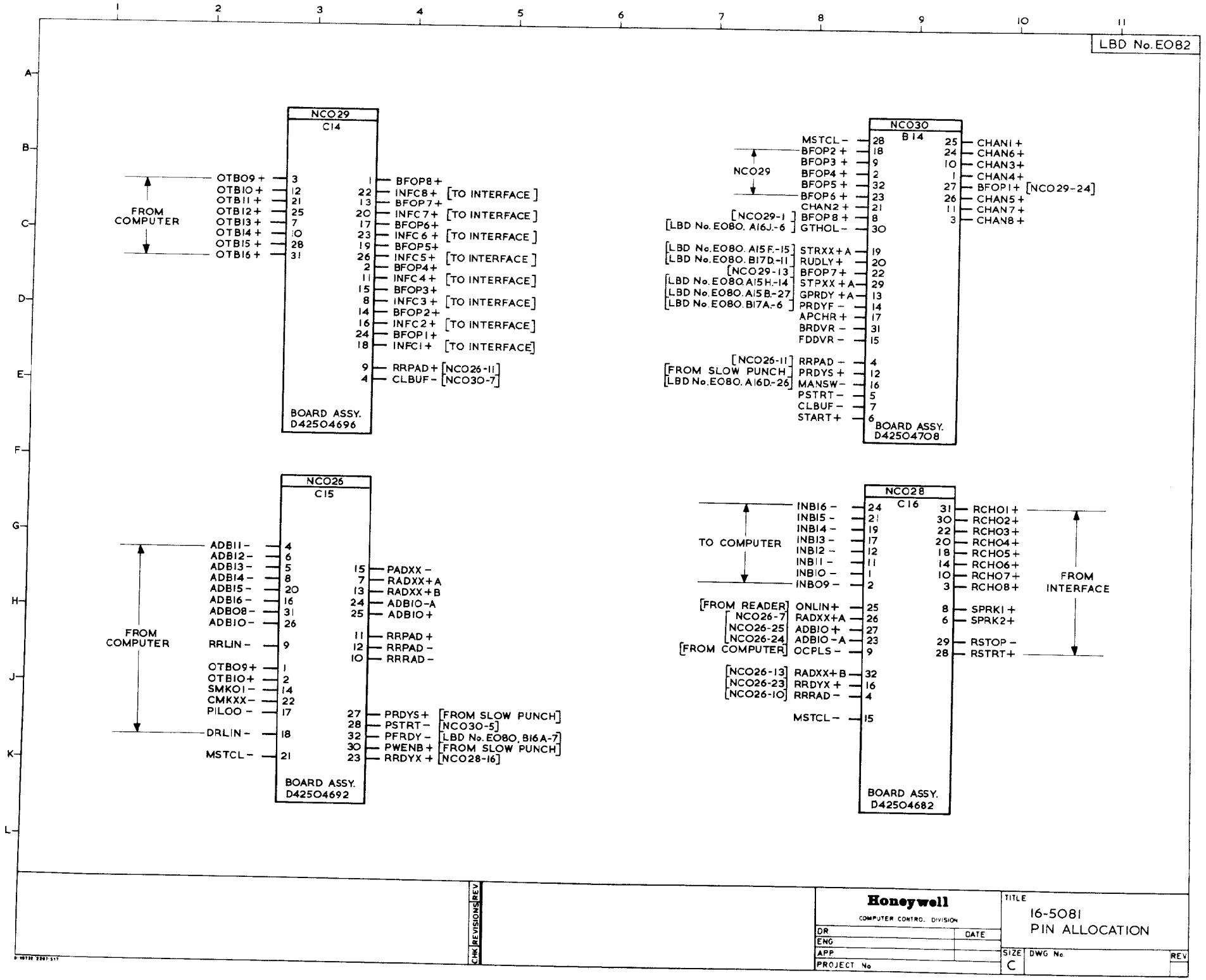
NCO29 PAC SCHEMATIC (C14)
PUNCH DATA BUFFER
SIZE C
DWG No.
REV
REVISIONS
CHK


LBD No E080
BTAPE –
BTAPE +
PRDYF +
MCOMB –
MCOMB +
MCOMB-A
BTAPE-A
TPOUT –
OSCOP –
INRDY +
INRDY –
PFRDY –
MANSW –
MANSW +
PRDYF –
(LBD No E082 NCO26)
RRPAD –
APCHR +
(LBD No E082 NCO30)
MSTCL –
OSCIP –
TO PUNCH
SIGMO +
SIGMO –
RLDVR +
RLDVR – (GND)
STRXX-A
STCTR –
STCTR +
RUDLY –
RUDLY +
RUDLY –
APCHR +
HOLES +
GTHOL –
(LBD No E082 NCO30)APCHR +
RSCTR –
(FROM PUNCH) OSCOP –
OSCOP +
PRDYF +
OSCRS –
STRXX +
STRXX –
STRXX+A
STPXX +
STPXX –
STPXX+A
GPRDY +
GPRDY –
GPRDY+A
BRDVR –
BRDVR +
FDDVR –
FDDVR +
LBD No E082 NCO30
TO PUNCH
CHAN1 +
CHAN2 +
CHAN3 +
CHAN4 +
CHAN5 +
CHAN6 +
CHAN7 +
CHAN8 +
DTDO1 +
DTDO1 –
DTDO2 +
DTDO2 –
DTDO3 +
DTDO3 –
DTDO4 +
DTDO4 –
DTDO5 +
DTDO5 –
DTDO6 +
DTDO6 –
DTDO7 +
DTDO7 –
DTDO8 +
DTDO8 –
LBD No E082 NCO30
TO PUNCH
Honeywell
COMPUTER CONTROL DIVISION
DR
ENG
APP
PROJECT No
DATE
TITLE
ADDITIONAL PACS FOR HIGH SPEED PUNCH GATING AND CONTROL.
SIZE C
DWG No
REV
CHK
REVISIONS
REV


LBD No. E081
A11
MCOMB – 1 2 DTDO8+
PWENB+ 3 4 DTDO8–
DTDO7+ 5 6 STPXX+
DTDO7– 7 8 DTDO6+
STRXX+ 9 10 DTDO6–
DTDO5+ 11 12 OSCIP–
DTDO5– 13 14 DTDO4+
GPRDY+ 15 16 DTDO4–
DTDO3+ 17 18 BRDVR+
DTDO3– 19 20 DTDO2+
FDDVR+ 21 22 DTDO2–
DTDOI+ 23 24 OSCOP–
DTDOI– 25 26 RLDVR+
BTAPE– 27 28 TPOUT–
29 30 VOLT 6+
GND 31 32
B11
OTBO9+ 1 2 INBO9–
INBIO– 3 4 ADBI2–
ADBI3– 5 6 OTBIO+
OTBII+ 7 8 INBII–
INBI2– 9 10 ADBI4–
ADBI5– 11 12 OTBI2+
OTBI3+ 13 14 INBI3–
INBI4– 15 16 ADBI6–
PILOO– 17 18 OTBI4+
OTBI5+ 19 20 INBI5–
INBI6– 21 22 SPARE+B
PWRFL– 23 24 OTBI6+
CMKXX– 25 26 VDCOO-E
SPARE+C 27 28 VDCOO-F
RRLIN– 29 30 VDCO6-A
MSTCL– 31 32 VDCO6-B
C11
OTBOI+ 1 2 INBOI–
INBO2– 3 4 ADBO7–
ADBO8– 5 6 OTBO2+
OTBO3+ 7 8 INBO3–
INBO4– 9 10 ADBO9–
ADBIO– 11 12 OTBO4+
OTBO5+ 13 14 INBO5–
INBO6– 15 16 ADBII–
DRLIN– 17 18 OTBO6+
OTBO7+ 19 20 INBO7–
INBO8– 21 22 PARCK–
SPARE+A 23 24 OTBO8+
SMKXX+ 25 26 VDCOO-A
OCPLS– 27 28 VDCOO-B
SMKOI– 29 30 VDCOO-C
ERLXX– 31 32 VDCOO-D
C17
RCHOI+ 1 2 RCHO2+
RCHO3+ 3 4 RCHO4+
RCHO5+ 5 6 RCHO6+
RCHO7+ 7 8 RCHO8+
9 10
SPRK2+ 11 12 RSTRT+
SPRKI+ 13 14 RSTOP+
ONLIN+ 15 16
17 18
19 20
21 22
23 24
25 26
27 28
29 30
GND 31 32
1 2
3 4
5 6
7 8
9 10
11 12
13 14
15 16
17 18
19 20
21 22
23 24
25 26
27 28
29 30
31 32
NOTES
1. A11 PIN 3, A17 PIN 25 AND A17 PIN 23 ARE CONNECTED TOGETHER.
2. THE HIGH SPEED PUNCH PWENB+ SIGNAL IS INPUT ON A11 PIN 3. THE SLOW SPEED PUNCH PWENB+ SIGNAL IS INPUT ON A17 PIN 25 (PNCH6+).
A17
INFC6+ 1 2
3 4
PRDYS+ 5 6 INFC3+
7 8
9 10
11 12 INFC4+
START+ 13 14
15 16
INFC8+ 17 18 INFC5+
19 20
21 22
PWENB+ 23 24 INFCI+
PNCH6+ 25 26
PCHSD– 27 28
INFC7+ 29 30 INFC2+
GND 31 32
B18
OTBO9+ 1 2 INBO9–
INBIO– 3 4 ADBI2–
ADBI3– 5 6 OTBIO+
OTBII+ 7 8 INBII–
INBI2– 9 10 ADBI4–
ADBI5– 11 12 OTBI2+
OTBI3+ 13 14 INBI3–
INBI4– 15 16 ADBI6–
PILOO– 17 18 OTBI4+
OTBI5+ 19 20 INBI5–
INBI6– 21 22 SPARE+B
PWRFL– 23 24 OTBI6+
CMKXX– 25 26 VDCOO-E
SPARE+C 27 28 VDCOO-F
RRLIN– 29 30 VDCO6-A
MSTCL– 31 32 VDCO6-B
C18
OTBOI+ 1 2 INBOI–
INBO2– 3 4 ADBO7–
ADBO8– 5 6 OTBO2+
OTBO3+ 7 8 INBO3–
INBO4– 9 10 ADBO9–
ADBIO– 11 12 OTBO4+
OTBO5+ 13 14 INBO5–
INBO6– 15 16 ADBII–
DRLIN– 17 18 OTBO6+
OTBO7+ 19 20 INBO7–
INBO8– 21 22 PARCK–
SPARE+A 23 24 OTBO8+
SMKXX– 25 26 VDCOO-A
OCPLS– 27 28 VDCOO-B
SMKOI– 29 30 VDCOO-C
ERLXX– 31 32 VDCOO-D
1 2
3 4
5 6
7 8
9 10
11 12
13 14
15 16
17 18
19 20
21 22
23 24
25 26
27 28
29 30
31 32
CHK REVISIONS REV
Honeywell
COMPUTER CONTROL DIVISION
DR DATE
ENG
APP
PROJECT No
TITLE
16-5081
OPTION CONNECTORS
SIZE C
DWG No
REV


LBD No. E082
NCO29
C14
FROM COMPUTER
OTB09+ 3
OTB10+ 12
OTB11+ 21
OTB12+ 25
OTB13+ 7
OTB14+ 10
OTB15+ 28
OTB16+ 31
1 BFOP8+
22 INFC8+ [TO INTERFACE]
13 BFOP7+
20 INFC7+ [TO INTERFACE]
17 BFOP6+
23 INFC6+ [TO INTERFACE]
19 BFOP5+
26 INFC5+ [TO INTERFACE]
2 BFOP4+
11 INFC4+ [TO INTERFACE]
15 BFOP3+
8 INFC3+ [TO INTERFACE]
14 BFOP2+
16 INFC2+ [TO INTERFACE]
24 BFOP1+
18 INFC1+ [TO INTERFACE]
9 RRPAD+ [NCO26-11]
4 CLBUF- [NCO30-7]
BOARD ASSY. D42504696
NCO30
B14
NCO29
MSTCL- 28
BFOP2+ 18
BFOP3+ 9
BFOP4+ 2
BFOP5+ 32
BFOP6+ 23
CHAN2+ 21
[NCO29-1] [LBD No. E080. A16J.-6] BFOP8+ 8
GTHOL- 30
[LBD No. E080. A15F.-15] [LBD No. E080. B17D.-11] STRXX+A 19
RUDLY+ 20
[NCO29-13] BFOP7+ 22
[LBD No. E080. A15H.-14] STPXX+A 29
[LBD No. E080. A15B.-27] GPRDY+A 13
[LBD No. E080. B17A.-6] PRDYF- 14
APCHR+ 17
BRDVR- 31
FDDVR- 15
[NCO26-11] RRPAD- 4
[FROM SLOW PUNCH] PRDYS+ 12
[LBD No. E080. A16D.-26] MANSW- 16
PSTRT- 5
CLBUF- 7
START+ 6
25 CHAN1+
24 CHAN6+
10 CHAN3+
1 CHAN4+
27 BFOP1+ [NCO29-24]
26 CHAN5+
11 CHAN7+
3 CHAN8+
BOARD ASSY. D42504708
NCO26
C15
FROM COMPUTER
ADBI1- 4
ADBI2- 6
ADBI3- 5
ADBI4- 8
ADBI5- 20
ADBI6- 16
ADBO8- 31
ADBI0- 26
RRLIN- 9
OTBO9+ 1
OTBI0+ 2
SMKOI- 14
CMKXX- 22
PILOO- 17
DRLIN- 18
MSTCL- 21
15 PADXX-
7 RADXX+A
13 RADXX+B
24 ADBIO-A
25 ADBIO+
11 RRPAD+
12 RRPAD-
10 RRRAD-
27 PRDYS+ [FROM SLOW PUNCH]
28 PSTRT- [NCO30-5]
32 PFRDY- [LBD No. E080, B16A-7]
30 PWENB+ [FROM SLOW PUNCH]
23 RRDYX+ [NCO28-16]
BOARD ASSY. D42504692
NCO28
C16
TO COMPUTER
INBI6- 24
INBI5- 21
INBI4- 19
INBI3- 17
INBI2- 12
INBI1- 11
INBI0- 1
INBO9- 2
[FROM READER] [NCO26-7] [NCO26-25] [NCO26-24] ONLIN+ 25
RADXX+A 26
ADBIO+ 27
ADBIO-A 23
[FROM COMPUTER] OCPLS- 9
[NCO26-13] [NCO26-23] [NCO26-10] RADXX+B 32
RRDYX+ 16
RRRAD- 4
MSTCL- 15
31 RCHO1+
30 RCHO2+
22 RCHO3+
20 RCHO4+
18 RCHO5+
14 RCHO6+
10 RCHO7+
3 RCHO8+
8 SPRK1+
6 SPRK2+
29 RSTOP-
28 RSTRT+
FROM INTERFACE
BOARD ASSY. D42504682
CHK REVISIONS REV
Honeywell
COMPUTER CONTROL DIVISION
DR DATE
ENG
APP
PROJECT No
TITLE
16-5081
PIN ALLOCATION
SIZE C
DWG No.
REV

LBD No. E083

LOC	PAC	A	B	C	D	E	F	G	H	J	K	L	M	N	P
8															
7	CONN			5	0	8	5	PUNCH							
6	DI 335	X	X	X	X	X	X	X	X	X	X				
5	DI 335	X	X	X	X	X	X	X	X	X	X				
4	BC 337	X													
3	CCO55	X	X	X	X										
2															
1	CONN			5	0	8	6	PUNCH							

A

LOC	PAC	A	B	C	D	E	F	G	H	J	K	L	M	N	P
8	CONN				1/O										
7	FA 335	X	X	X											
6	PA 336	X	X	X											
5															
4	NCO3O														
3	CCO55	X	X	X	X										
2															
1	CONN				1/O										

B

LOC	PAC	A	B	C	D	E	F	G	H	J	K	L	M	N	P
8	CONN	X			1/O										
7	CONN			5	0	8	2	READER							
6	NCO28														
5	NCO26														
4	NCO29														
3	CCO55	X													
2															
1	CONN				1/O										

C

△1 REQUIRED FOR FACIT 4060 HIGH SPEED PUNCH (5086)
△2 REQUIRED FOR FACIT 4070 LOW SPEED PUNCH (5085)
△3 REQUIRED FOR HONEYWELL PAPER TAPE READER (5082)
△4 REQUIRED FOR ALL APPLICATIONS (5081)

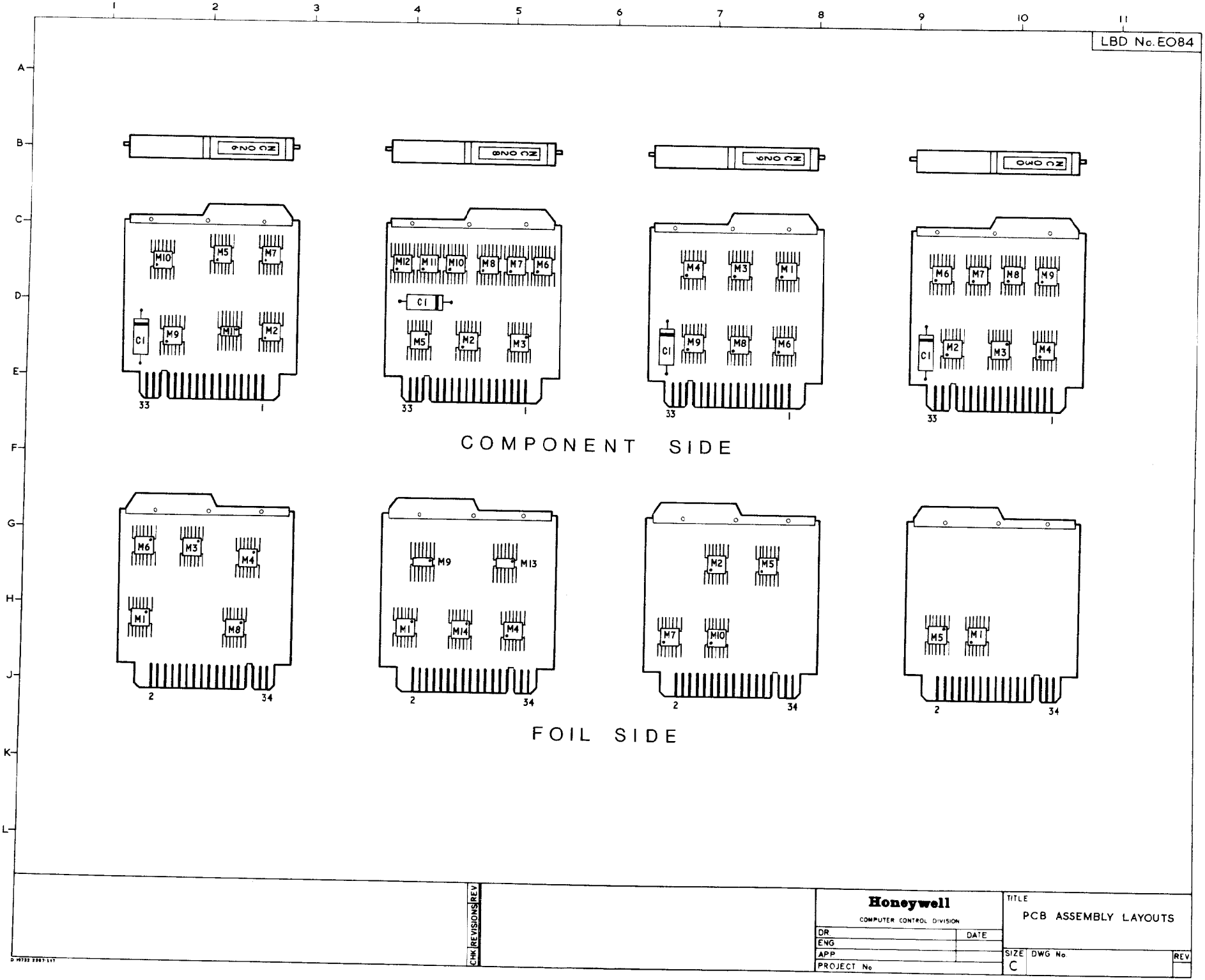
AS VIEWED FROM READER

REV	REVISIONS	CHK

Honeywell
COMPUTER CONTROL DIVISION

	DATE
DR	
ENG	
APP	
PROJECT No.	

TITLE: 16-5081 PAC ALLOCATION CHART
SIZE: C
DWG No.
REV



PCB Assembly Layouts

USERS REMARKS FORM

Title: Series 16 - 5081 Paper Tape Reader/ Punch Controller

Dated: September, 1970

Part No: 42401026-001

Errors/Suggestions:

Cut Along Line

(Please Print)

From: Name _____ Date: _____

Company _____

Title _____

Address _____

_____

On completion return to: HONEYWELL LIMITED,
GREAT WEST HOUSE,
GREAT WEST ROAD,
BRENTFORD,
MIDDLESEX,
ENGLAND.

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