Series 16

HARDWARE DOCUMENTATION

DDP-516
Paper Tape Reader Option
Model 516-50/9550

INSTRUCTION MANUAL

This manual contains a description of the DDP-516 Paper Tape Reader Option, Model 516-50/9550, and its operation. A parts list, logic block diagrams, and special circuit module descriptions are included.

DOC.NO. 130071642F ■ ORDER NO. M-973 ■ OCT. 1970

Honeywell

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New Revision Level of Manual	Change No.	Effective Date	Number and New Revision Level of Affected Drawings	Pages Affected by Revision
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D	5608	June 1968	015357E	7/8 17/18
E	5609	Aug. 1968	015353E 015354E	9/10 11/12 A-1; Deleted CC-060 and CC-127 PACs
F	5714	Oct. 1968	015353F 015354F	9/10 11/12 5 7/8 A-1: Add CC-272 PAC

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DDP-516-50
PAPER TAPE READER

INTRODUCTION

The DDP-516-50 Paper Tape Reader Option consists of an unmodified Digitronics Perforated Tape Reader (Model 2500) and one 1 x 3 assembly of interface logic linking the paper tape reader to the main frame of the DDP-516 General Purpose Computer. This document provides technical information on the interface logic.

Reference Data

The following manuals are recommended for supplementary reference:

Technical Manual, Perforated Tape Reader, Model 2500 (Digitronics Corp.)

Programmers Reference Manual for the DDP-516 General Purpose Computer, 3C Doc. No. 130071585

Interface Manual for DDP-516 General Purpose Computer, 3C Doc. No. 130071624

Installation Manual for DDP-516 General Purpose Computer, 3C Doc. No. 130071625

Instruction Manual for μ-PAC Integrated Circuit Modules, 3C Doc. No. 130071369

Physical Characteristics

The paper tape reader is 10 in. wide and 6 in. high. It extends 10-5/8 in. behind the front panel and 2-3/8 in. in front of the panel. The reader weighs approximately 15 lb and is secured to a rack mount adapter panel for mounting in the 3C Paper Tape Equipment Cabinet. The reader is linked to the control module logic BLOC by a control cable with a maximum permissible length of 50 ft. (LBD No. 0.303). The interface logic BLOC mounts in any available BLOC location in a DDP-516 or satellite cabinet.

Functional Description

The paper tape reader is unidirectional and reads eight-level tape continuously at a slewing rate of 300 characters per second. When operated in an asynchronous start/stop mode, the reader is capable of stopping on the next character at a maximum slew rate of 300 characters per second. All eight data levels are read from the tape to the device buffer and transferred intact to the DDP-516 input data bus. Tape leader characters are transferred as an all ZERO configuration.

For additional information, refer to the Programmers Reference Manual for DDP-516 General Purpose Computer, 3C Doc. No. 130071585.

Tape Format

The paper tape reader uses standard 8-level tape punched in the format shown on Figure 1.

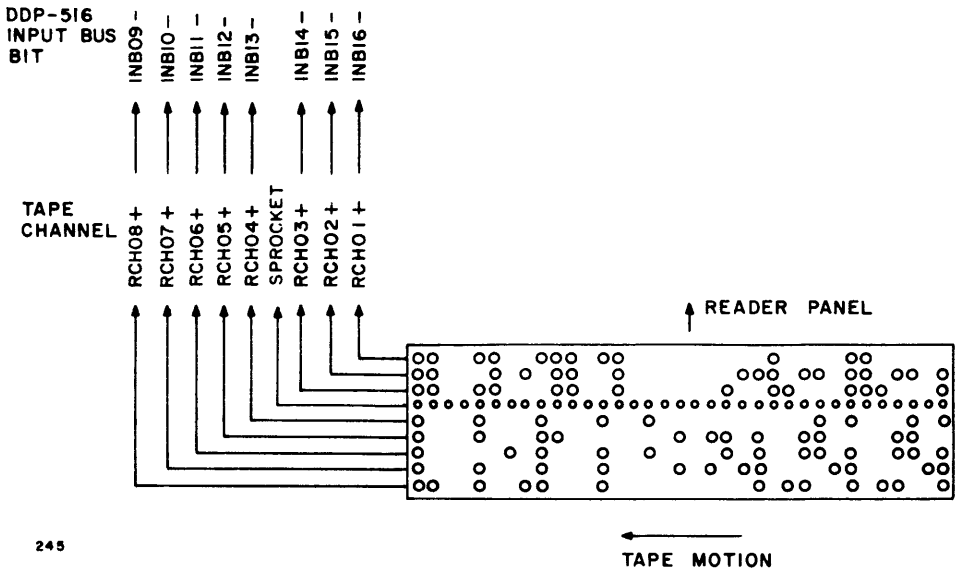


Figure 1. Tape Format

Power Requirements

The DDP-516-50 paper tape reader requires 105 Vac to 125 Vac, single phase, 60 Hz at 125 W. The DDP-516-9550 requires 105 Vac to 125 Vac, single phase, 50 Hz at 125 W.

Operation

Operating instructions for the paper tape reader are given in the Technical Manual for Paper Tape Reader, Model 2500 (Digitronics Corp.) and in the Programmers Reference Manual for the DDP-516 General Purpose Computer, 3C Doc. No. 130071585.

Maintenance

The paper tape reader data channels may require alignment and the pinch roller should be checked periodically. Refer to the technical manual for Digitronics Perforated Tape Reader for the maintenance procedures and recommended period of inspection and preventive maintenance. The interface requires no special maintenance.

INSTALLATION

Connector and PAC Layout

The paper tape reader mechanism mounts in a special paper tape equipment cabinet and the interface logic is contained within a standard 1 x 3 μ-BLOC. Connector and PAC locations within the BLOC are as shown on LBD No. 0.304 and connector pin assignments are shown on LBD No. 0.302.

Interface Connections

The DDP-516 I/O bus and the paper tape reader are connected through cable μ-PACs. Signal name and pin connections are shown on the logic diagrams. Pin assignments between the paper tape reader connector and the interface cable μ-PAC are shown on LBD No. 0.303. All wires are number 24 red/black twisted pairs, and can have a maximum length of 50 ft.

THEORY OF OPERATION

In general operation, the paper tape reader responds to two OCP functions: reader start and reader stop. When the reader is started, data characters are dropped into an 8-bit buffer register and stored until an input data transfer to the DDP-516 is accomplished. The tape slews at a speed which causes a new character to be dropped into the register every 3.3 ms. Input data transfer is accomplished by an INA instruction.

A standard interrupt provision is included as part of the interface, with the mask flip-flop responding to bit nine on the output bus.

The main subdivisions of interface logic and the data and control lines exchanged with the DDP-516 and reader mechanism are shown on Figure 2. An analysis of the paper tape reader interface logic is presented in the following paragraphs. The timing of tape reader data cycles is illustrated in Figure 3 and definitions of mnemonics are contained in Table 1.

Run Command

When OCP '0001 is detected by the coincidence of 0CPXX+, ADB10-A, and RADXX+A, the run/stop flip-flop is set. The assertion output of the flip-flop is powered through a parallel NAND gate structure and level shifter to produce -6v on the RNSTP+ line to the reader mechanism. The reader brake disengages, the pinch roller engages, and the tape begins to slew.

Time A

Time A starts with tape motion (see Figure 3). The interface waits for synchronization with the paper tape reader sprocket signal (RSHXX+). When a sprocket hole passes over the sprocket channel photodiode, a negative-going RSHXX+ sprocket pulse is generated. Time A is terminated with the leading edge of RSHXX+ which in turn starts time B. The next time A and every time A thereafter, until tape motion stops, is initiated with the leading edge of RRLAD-.

Time B

During time B, data is strobed by D1PXX+, through level converters, to the interface buffer register. The manner in which the DDP-516 accepts the character depends on whether standard interrupt or programmed I/O is in effect.

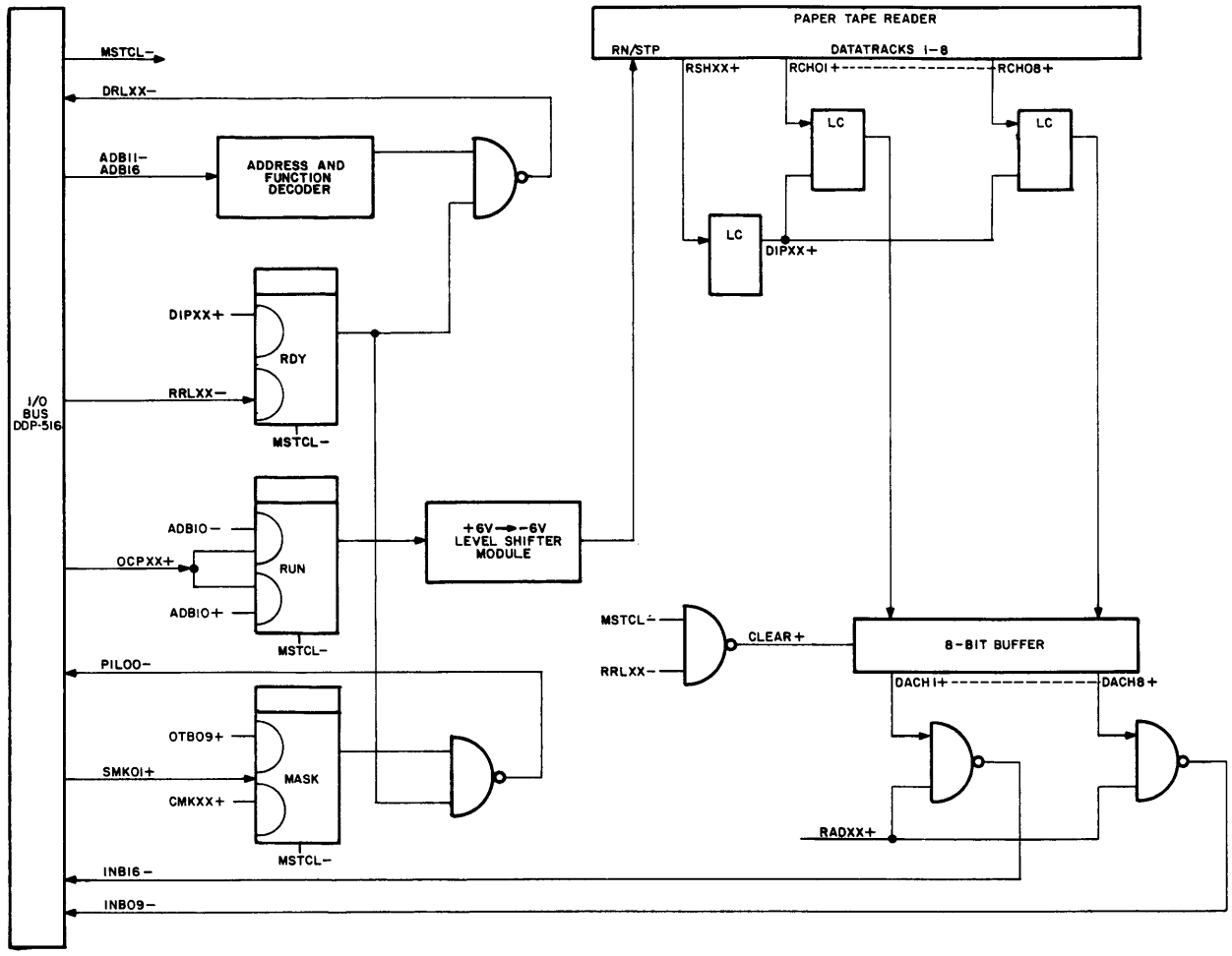


Figure 2. Tape Reader Interface, Block Diagram

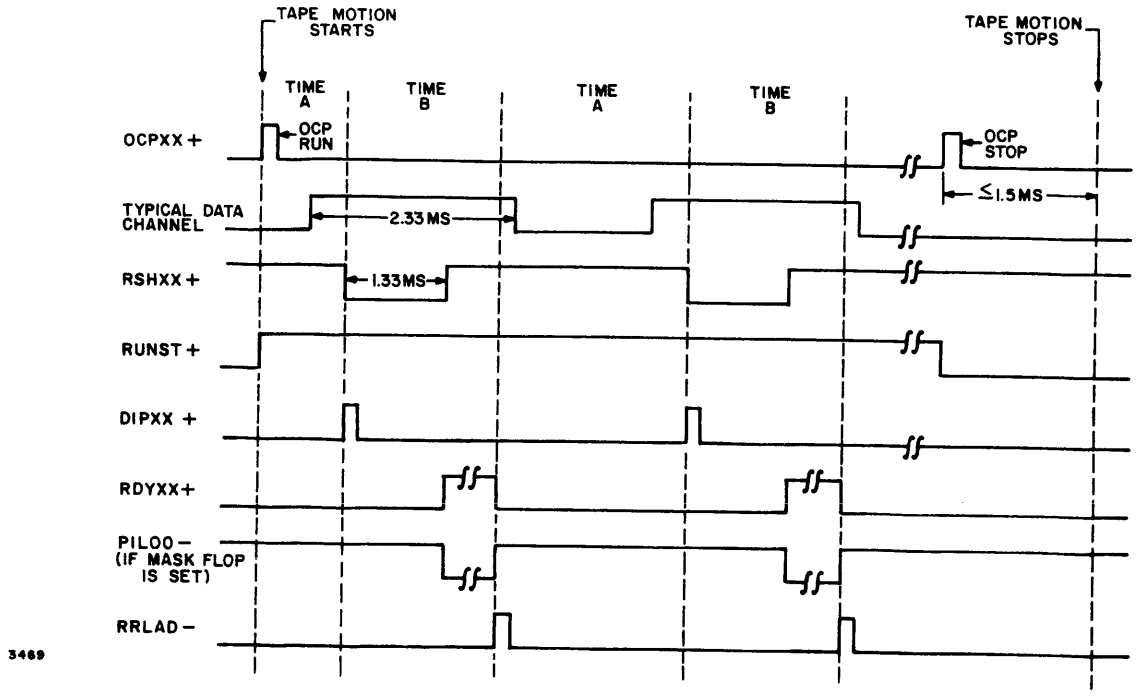


Figure 3. Tape Reader Interface Timing

If standard interrupt is being used and the mask flip-flop is set, the ready flip-flop causes the P1L00- priority interrupt line to go to ground. If the DDP-516 performs an SKS '0401, the presence of 1NTXX- inhibits the DRL1N- line as an indication of an interrupt by the tape reader interface. This subsequently leads to the addressing of an INA '0001 or '1001 by the DDP-516 to transfer the contents of the reader buffer register into the DDP-516 A-register.

When an INA '0001 or '1001 is executed, either as a response to the P1L00- interrupt signal or in the course of a programmed I/O, the RRLAD- pulse is generated. This pulse resets the ready flip-flop, deenergizing P1L00-. For the duration of the device address, the RDADX+A and RDADX+B levels gate the contents of the buffer register to input bus lines 1NB09- through 1NB16-. During the RRL period, the DDP-516 accepts the data. At the leading edge of RRLAD-, the ready flip-flop (RDYXX+) is reset and the reset pulse CLEAR+ is generated to reset the buffer register. The interface then returns to time A to await the next sprocket signal.

Stop Command

If an OCP '0101 is received during time A (0CPXX+ gated with ADB10+A and RADXX+), the RUNST+ flip-flop is reset and the interface returns to the reset condition. The RNSTP+ level returns to ground, engaging the tape reader brake and disengaging the pinch roller. The tape stops within 1.5 ms after RNSTP+ returns to ground.

Table 1.
Function Index

Mnemonic	Definition	LBD/Zone
CLEAR+	Reader clear pulse. Developed from the system normalize, master clear or reset ready line pulse.	0.300 H10
CMKXX-A	Clear mask flip-flop	0.300 L10
D1PXX+A D1PXX+B	Drop-in pulse. Strobes the data from the reader into the buffer register.	0.300 E10/E11
P1L00-	Priority interrupt level. Signals computer that reader is interrupting.	0.300 L8
RADXX+A RADXX+B	Reader address.	0.300 C2/C3
RCH01+ through RCH08+	Reader data channels.	0.302
RDYXX+	Ready flip-flop. Set with the drop-in pulse and reset when the computer strobes the input bus.	0.300 F1
RMASK+	Mask status flip-flop for the standard interrupt line.	0.300 F8
RNSTP+	Run/stop to the paper tape reader.	0.300 K4
RRLAD-	Reset ready line pulse. Gated with the reader address.	0.300 B4
RSHXX+	Reader sprocket pulse.	0.302
SMK01+	Set mask flip-flop for standard interrupt.	0.302
ST0CP-	Reader stop pulse.	0.300 C5

PARTS LIST

Table 2 contains the replaceable parts for the Paper Tape Reader option. Component parts for the μ-PAC digital modules, unless stated otherwise in the description, will be found in the associated documents listed below:

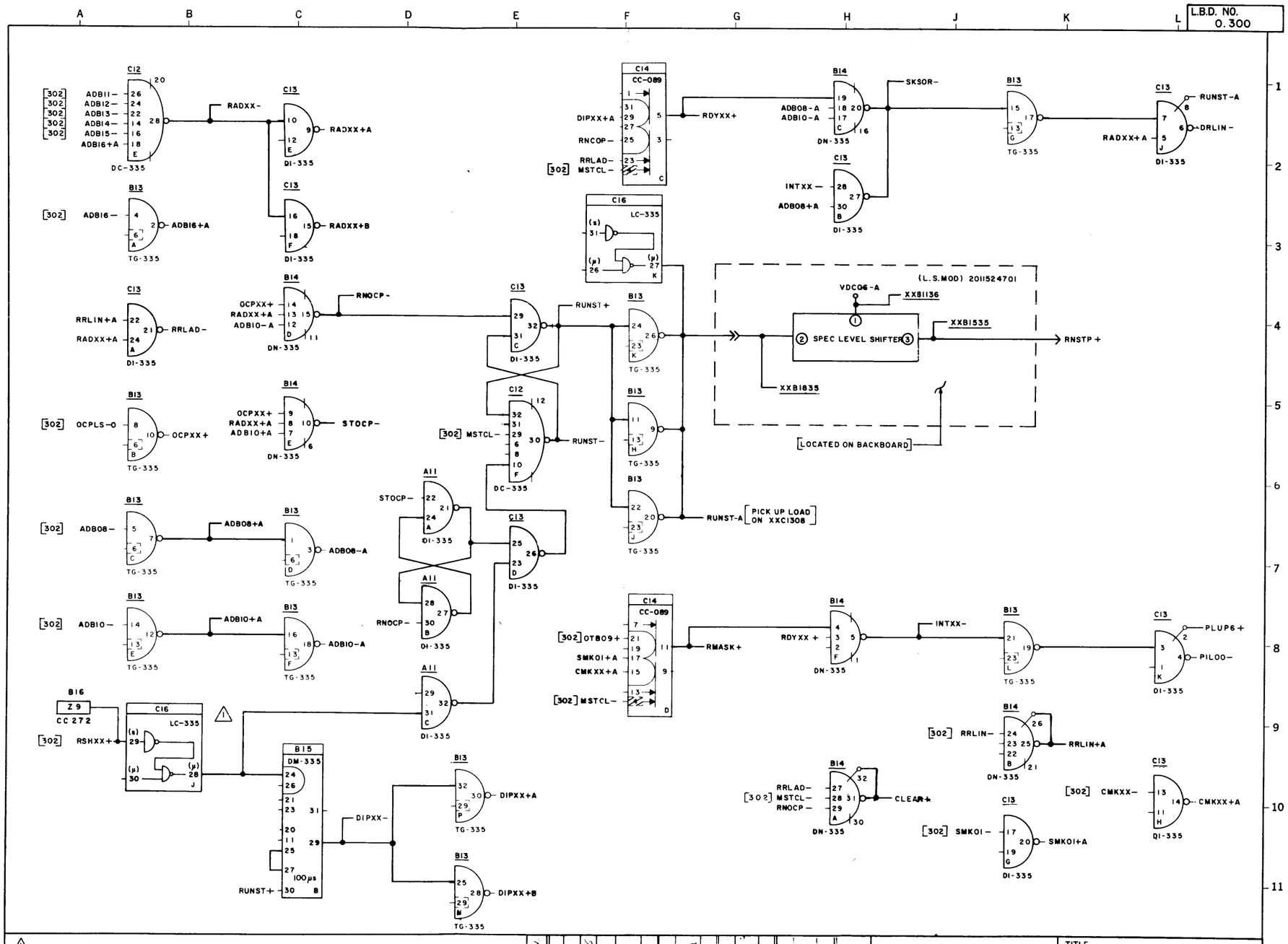
335 Series	Doc. No. 130071369
All others	Doc. No. 130071620

Reference (location) designations are variable and will be determined from the applicable system coding drawing.

Table 2.
Parts List for DDP-516-50 Paper Tape Reader

Reference Designation	Description	3C Part No.	Quantity Required
	TAPE READER--8 channels at 300 characters/second; unidirectional; panel mtd; DIGITRONICS Model 2500; for component parts refer to vendor's manual	964 500 001	1
	μ-PAC DIGITAL MODULE -- delay multivibrator	Model CC-060	1
	μ-PAC DIGITAL MODULE -- gated flip-flop	Model CC-089	1
	μ-PAC DIGITAL MODULE -- buffer register	Model CC-092	1
	μ-PAC DIGITAL MODULE -- diode resistor	Model CC-272	1
	μ-PAC DIGITAL MODULE -- transfer gate	Model CC-152	1
	μ-PAC DIGITAL MODULE -- multi-input NAND gate	Model DC-335	1
	μ-PAC DIGITAL MODULE -- NAND gate Type 1	Model DI-335	2
	μ-PAC DIGITAL MODULE -- expandable NAND gate	Model DN-335	1
	μ-PAC DIGITAL MODULE -- negative logic level converter; for component parts refer to 3C Doc. No. 130071620	Model LC-335	1
	μ-PAC DIGITAL MODULE -- transfer gate	Model TG-335	1
	CONNECTOR PLANE ASSY -- c/o one 1 x 3 connector block, special level shift module and associated parts; except for module factory repairable only	1015389-701	1
	LEVEL SHIFT MODULE -- c/o printed wiring board, diode and resistor; 3-wire pin terminals; o/a dim. 0.150 in. w by 0.305 in. max h by 1.835 in. lg excl terminals	2011608-701	1
	PRINTED WIRING BOARD -- etched wiring one side	2011522-001	1
	RESISTOR, COMPOSITION -- 910 ohms, 5%, 1/2w; MIL Type RC20GF911J	932 004 048	1
	SEMICONDUCTOR, DIODE -- 1N705A	943 102 010	1
	CABLE ASSY, SPECIAL PURPOSE -- c/o 10-pairs cabled and covered w/insulating sleeve; one end printed wiring board; other end 23-pin connector; o/a length 50 ft	1015331-701	1
	PRINTED WIRING BOARD -- μ-PAC configuration w/o components; incl cable clamp, clamping bar and plate	2013625-701	1
	CONNECTOR, PLUG -- 23 female contacts; incl jackscrews and rt ang cable clamp; U.S. COMPONENTS UPCC-F-2HSL-23	--	1
	CABLE, SPECIAL PURPOSE -- twisted pair; #24 AWG; stranded conductors w/plastic insulation	940 352 001	500 ft
	CABINET, ELECTRICAL EQUIPMENT -- provides external mounting for both tape reader and/or tape punch (516-52 option); configuration and finish color to be specified by system requirements		1

L.B.D. NO. 0.300



⚠ ALL INPUTS TO LC-335(S) PIN ARE LOGICALLY DEFINED AS TRUE AT -10V AND FALSE AT GROUND

REV.	REVISIONS	CHK
B	ECO 3718 REDRAWN	
C	ECO 3991 EXT. CHANGES 1/31/67	RD
D	ECO 4239 EXT CHNG. SEE ECO 10-5-68 D.M.H.	
E	ECO 5609 EXT. CHANGES 8/9/68 A.K.	
F	ECO 5741 EXT. CHANGES 10/2/68 P.B.	

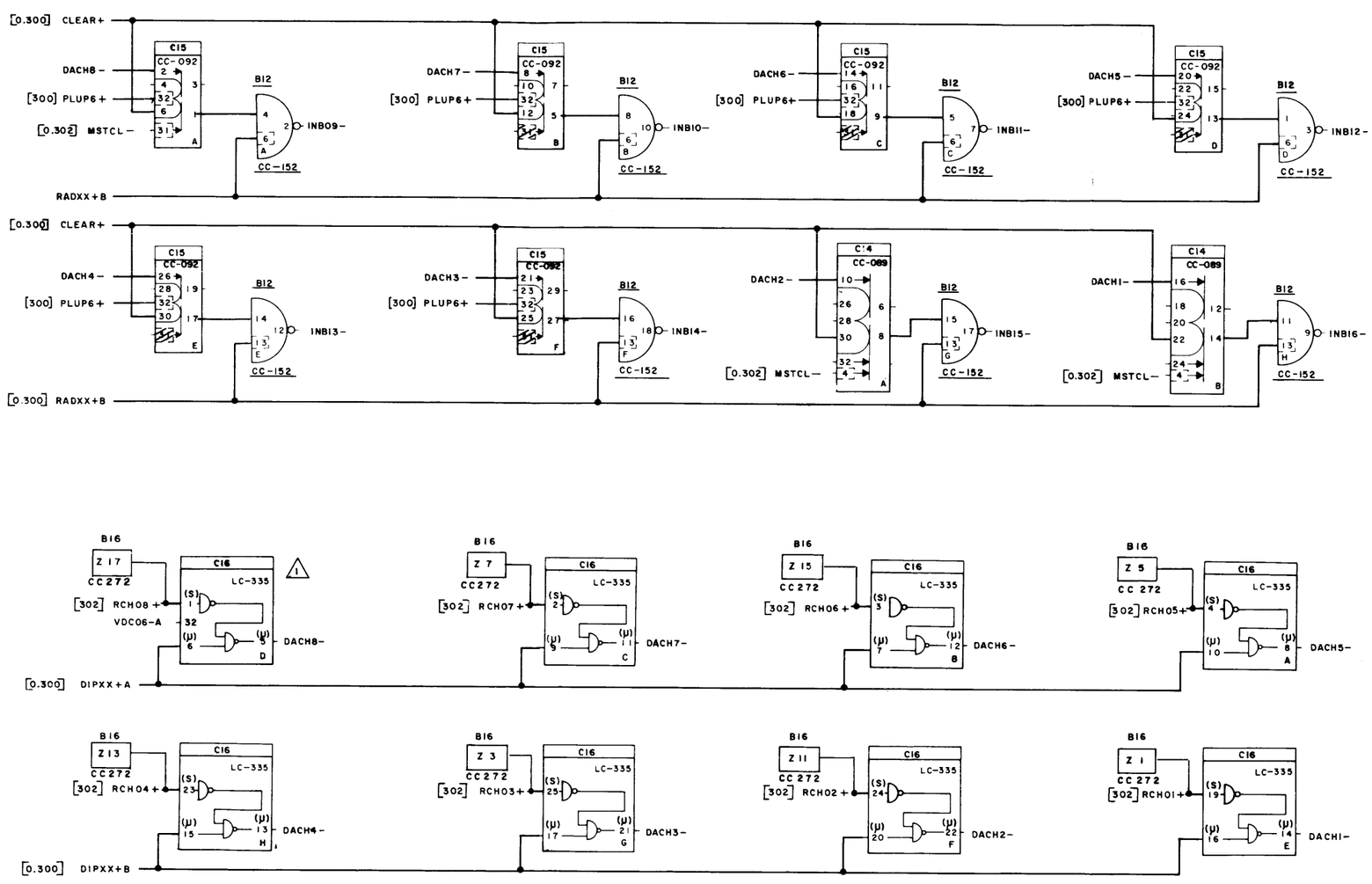
HONEYWELL INC.
COMPUTER CONTROL DIVISION
Old Connecticut Path, Framingham, Mass.

DR.	A. KURTZER	DATE 7/7/66
ENG.	J. THAXTER	7/29/66
APP.	G. C. HENDRIE	8/2/66
PROJECT NO.	55242	

TITLE
PAPER TAPE READER CONTROL
DDP-516-50

SIZE C | DWG NO. 015353 | REV. F

L.B.D. NO. 0.301



△1 REFER TO NOTE △1 ON LBD 0.300

REV.	REVISIONS	CHK
B	ECO 3718 * REDRAWN	
C	ECO 3991 EXT. CHANGES 1/31/67	
D	ECO 4239 EXT. CHNG. SEE ECO 10-5-68	
E	ECO 5609 EXT. CHANGES 8/9/68	
F	ECO 5741 EXT. CHANGES 10/2/68	

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DR.	A. KURTZER	DATE 7/7/66
ENG.	J. THAXTER	7/29/66
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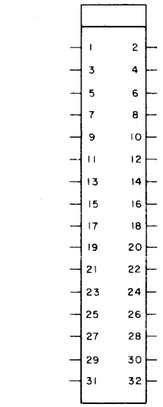
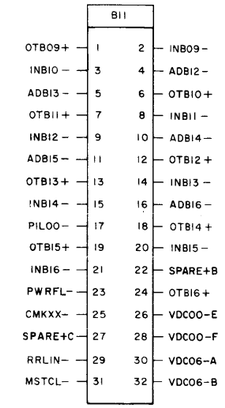
PROJECT NO.	55242	

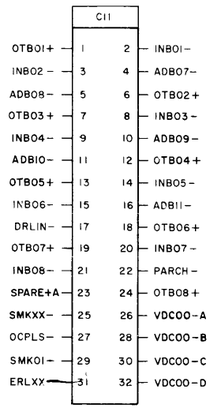
TITLE
PAPER TAPE READER
BUFFER REGISTERS
DDP-516-50

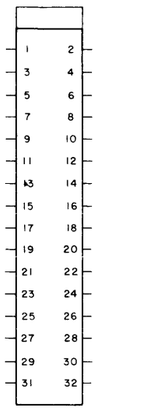
SIZE C | DWG NO. 015354 | REV. F

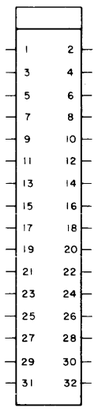
L.B.D. NO. 0.302

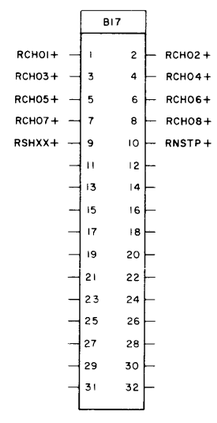


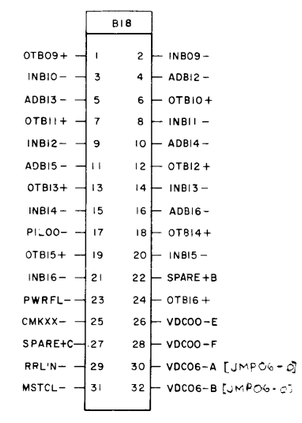


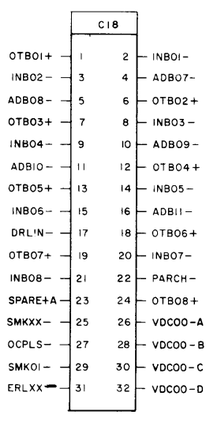


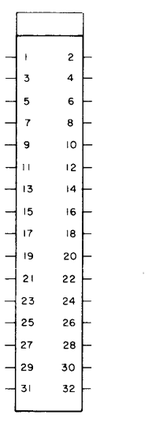


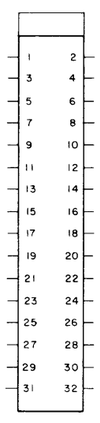












REVISIONS				
LTR	DESCRIPTION			
A	INITIAL RELEASE			
B	ECO 3991 EXT. CHANGES	1/31/67	JD	

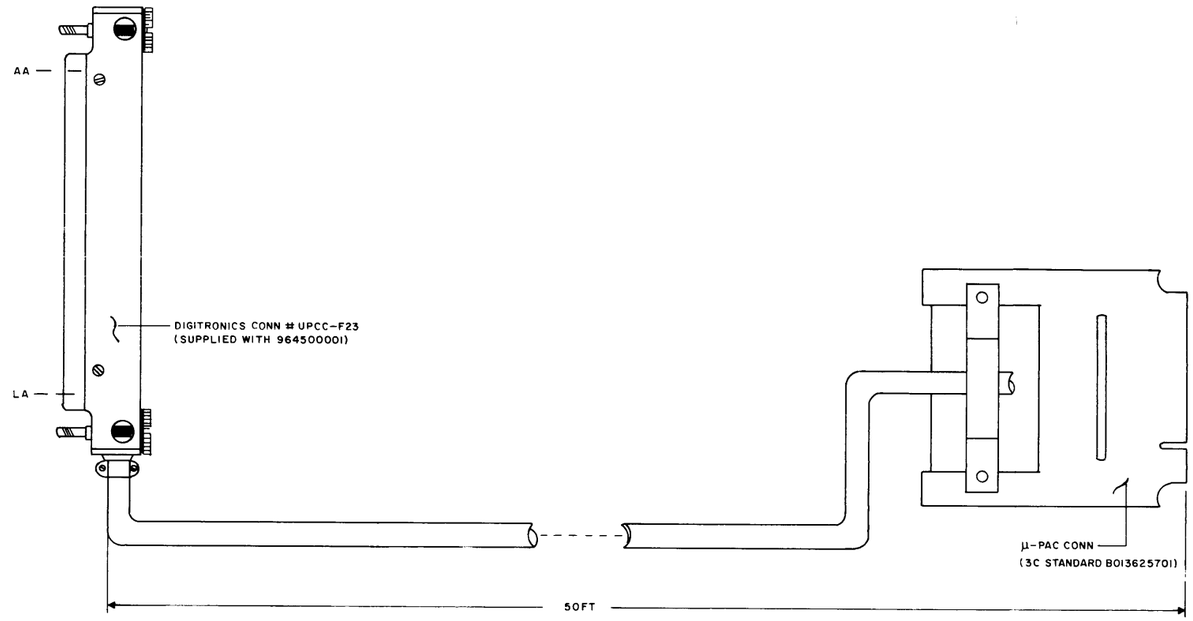
COMPUTER CONTROL COMPANY, INC
FRAMINGHAM, MASS. · LOS ANGELES, CALIF.

DR. RPB	DATE 7-29-66
ENG.	
APP.	8/2/66
PROJECT NO. 55542	

TITLE
CONNECTORS
PAPER TAPE READER
DDP-316-50

SIZE C | DWG NO. 015355 | REV. F

L.B.D. NO. 0.303



PAPER TAPE READER CABLE		
DEVICE		μ-PAC
LA	RCH01+	1
LB	RCH02+	2
LC	RCH03+	3
LD	RCH04+	4
LE	RCH05+	5
LF	RCH06+	6
LH	RCH07+	7
LJ	RCH08+	8
LV	RSHXX+	9
LY	RNSTP+	10
LK	GND	33
LZ	-15S	
AA	-15L	

REVISIONS

REV	ECO	CHK
B	3718	

REDRAWN BY: [illegible] 7/66

HONEYWELL INC.
COMPUTER CONTROL DIVISION
Old Connecticut Path, Framingham, Mass.

DR.	DATE
ENG. J. THAXTER	7/29/66
APP. G.C. HENDRIE	8/2/66
PROJECT NO. 55242	

TITLE
PAPER TAPE READER
DEVICE CABLE
DDP-516-50

SIZE C | DWG NO. 015356 | REV. B

L.B.D. NO. 304

A B C D E F G H J K L

4

LOC	PAC	A	B	C	D	E	F	G	H	J	K	L	M	N	P
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LOC	PAC	A	B	C	D	E	F	G	H	J	K	L	M	N	P
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LOC	PAC	A	B	C	D	E	F	G	H	J	K	L	M	N	P
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LOC	PAC	A	B	C	D	E	F	G	H	J	K	L	M	N	P
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LOC	PAC	A	B	C	D	E	F	G	H	J	K	L	M	N	P
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LOC	PAC	A	B	C	D	E	F	G	H	J	K	L	M	N	P
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LOC	PAC	A	B	C	D	E	F	G	H	J	K	L	M	N	P
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4															
3															
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LOC	PAC	A	B	C	D	E	F	G	H	J	K	L	M	N	P
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7															
6															
5															
4															
3															
2															
1															

LOC	PAC	A	B	C	D	E	F	G	H	J	K	L	M	N	P
8															
7															
6															
5															
4															
3															
2															
1															

1

A

LOC	PAC	A	B	C	D	E	F	G	H	J	K	L	M	N	P
8															
7															
6															
5															
4															
3															
2															
1	DI-335	X	X	X											

B

	LOC	PAC	A	B	C	D	E	F	G	H	J	K	L	M	N	P
△1	8	CONN														
△2	7	CONN														
	6															
	5	DM-335		X												
	4	DN-335	X	X	X	X	X	X								
	3	TG-335	X	X	X	X	X	X	X	X	X	X	X		X	X
	2	CC152	X	X	X	X	X	X	X	X						
△1	1	CONN														

L.S. MOD. 201-1524701

C

	LOC	PAC	A	B	C	D	E	F	G	H	J	K	L	M	N	P
△1	8	CONN														
	7															
	6	LC-335	X	X	X	X	X	X	X	X	X	X				
	5	CC092	X	X	X	X	X	X								
	4	CC089	X	X	X	X										
	3	DI-335	X	X	X		X	X	X	X	X	X				
	2	DC-335					X	X								
△1	1	CONN														

LOCATION XY.

NOTES:

△1 I/O BUS JUMPER CABLES

△2 DEVICE CABLE

REV	REVISIONS	CHK
A	TAKEN FROM S.R. 64-1241 8/1/66	
B	ECO 3991 EXT CHANGES 1/31/67	
C	ECO 4572 EXT. CHANGES SEE ECO 7/7/67	
D	ECO 4239 EXT. CHNG. SEE ECO 10-5-68 D.M.H.	
E	ECO 5608 EXT CHGS 6-4-68 A.K.	

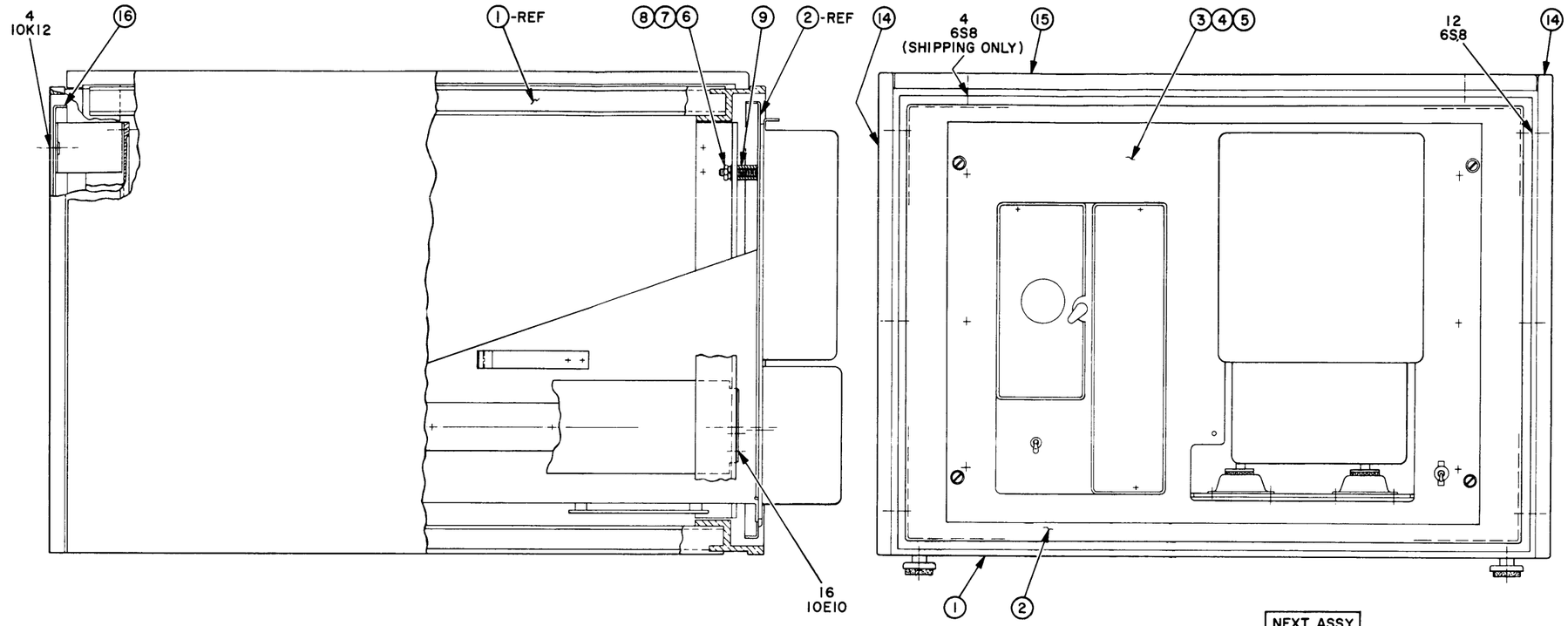
3C COMPUTER CONTROL COMPANY, INC.
FRAMINGHAM MASS / LOS ANGELES 64 CALIF

DR.		DATE
ENG.		7/29/66
APP.		

PROJECT NO. 55242

TITLE
PAC ALLOCATION
PAPER TAPE READER OPTION
DDP - 516-50

SIZE	DWG NO.	REV.
C	015357	E



C3770

701, 702, 703

1. ITEMS 14, 15 AND 16 SHOWN IN REFERENCE ONLY AND WILL BE CALLED FOR IN "PRODUCT INDEX" - DRAWING NO. A 015 031.
2. ITEMS 17 THRU 24 ARE NOT SHOWN. (FOR LOCATION AND MOUNTING HARDWARE SEE DRAWING NO. D015472.)

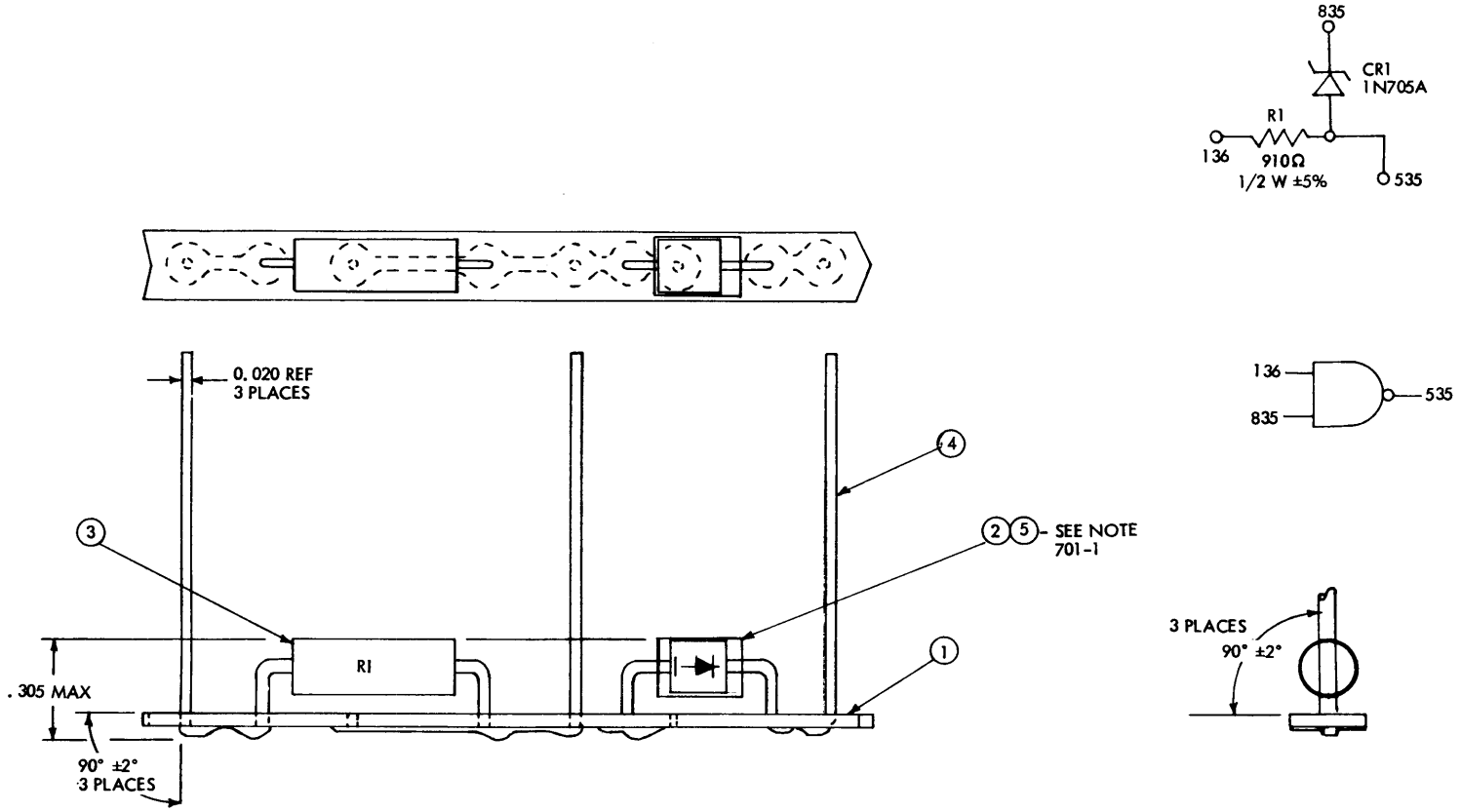
NEXT ASSY
A015031
A014298
A013805

APPENDIX
μ-PAC DESCRIPTIONS

This appendix contains the descriptions for the following.

	Level Shift Module (Dwg. No. B011524701)
CC-152	Transfer Gate PAC
CC-272	Diode Resistor PAC

Other PAC descriptions can be found at the end of the Instruction Manual for the DDP-516 General Purpose Computer, Volume I, 3C Doc. No. 130071620.



701

1. COVER ITEM 2 WITH ITEM 5 BEFORE INSTALLING TO ITEM 1.
2. ITEMS 2 AND 3 MAY BE MOUNTED FLUSH TO ITEM 1.

Dwg. No. B011524701 Printed Circuit Board Assembly Level Shift Module

TRANSFER GATE PAC, MODEL CC-152

The Transfer Gate PAC (Figure CC-152-1) contains 14 two-input NAND gates without collector resistors, arranged in four independent groups. Two of the groups contain four NAND gates each, with one input being common to the four gates. The other two groups contain three NAND gates each, with one input being common to the three gates. All 14 circuits provide a facility for connecting the NAND gates in parallel without decreasing the output drive capability.

The Model CC-152 PAC can be used for the common transfer control of up to 14 data signals, with the common input used as a control or strobe input. Turn-on rise time is controlled so as to have a guaranteed minimum of 50 ns with no load.

SPECIFICATIONS

Frequency of Operation

DC to 5 MHz (max)

Input Loading

Individual inputs: 1 unit load each

Common inputs: 1 unit load per gate

Output Drive Capability

8 unit loads

Circuit Delay

120 ns (max) turn-on
40 ns (max) turn-off

Current Requirements

+6V: 95 mA

Power Dissipation

560 mW (max)

Electrical Parts List

Ref. Desig.	Description	CCD Part No.
C1	CAPACITOR, FIXED, PLASTIC DIELECTRIC: 0.033 µF ±20%, 50 Vdc	930 313 016
C2-C15	CAPACITOR, FIXED, CERAMIC DIELECTRIC: 10 pF ±10%, 100 Vdc	930 173 204
M1-M7	MICROCIRCUIT: F-01 dual NAND gate integrated circuit	950 100 001

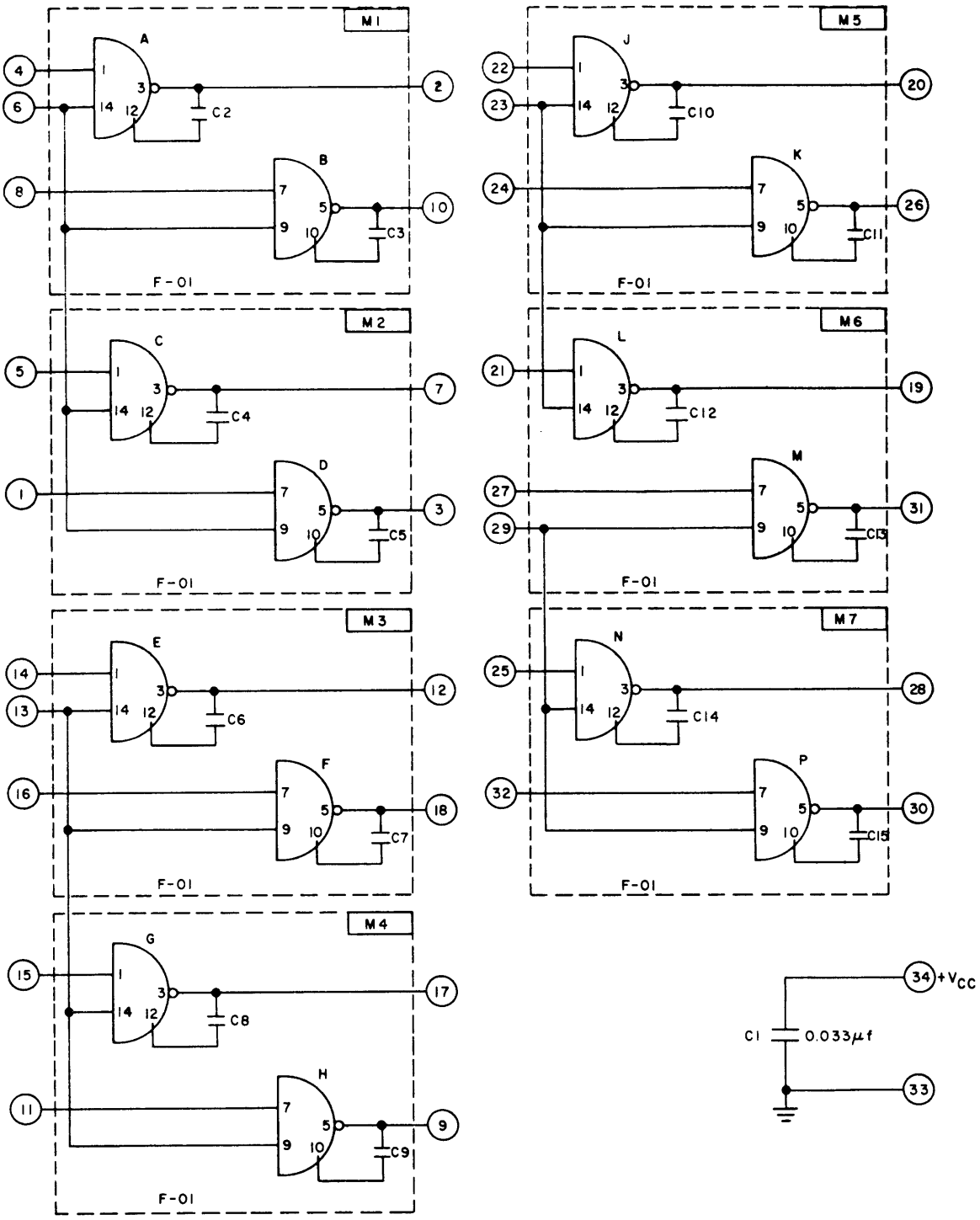


Figure CC-152-1. Transfer Gate PAC, Model CC-152, Schematic Diagram

DIODE RESISTOR PAC, MODEL CC-272

The Diode Resistor PAC, Model CC-272 (Figure CC-272-1), contains sixteen silicon diodes having common cathodes and anodes which are brought out to individual pins. There are also fourteen resistors (1K) which are pulled up to +Vcc.

SPECIFICATIONS

Current Requirements

80 mA (max) from Vcc = 5V

Electrical Parts List

Ref. Desig.	Description	CCD Part No.
R1-R14	RESISTOR FIXED COMPOSITION: 1K, 5%, 1/4W	932 007 049
CR1-CR16	DIODE SILICON	943 083 002
C1	CAPACITOR FIXED PLASTIC: 0.033 μF .±20% 50V	930 313 016

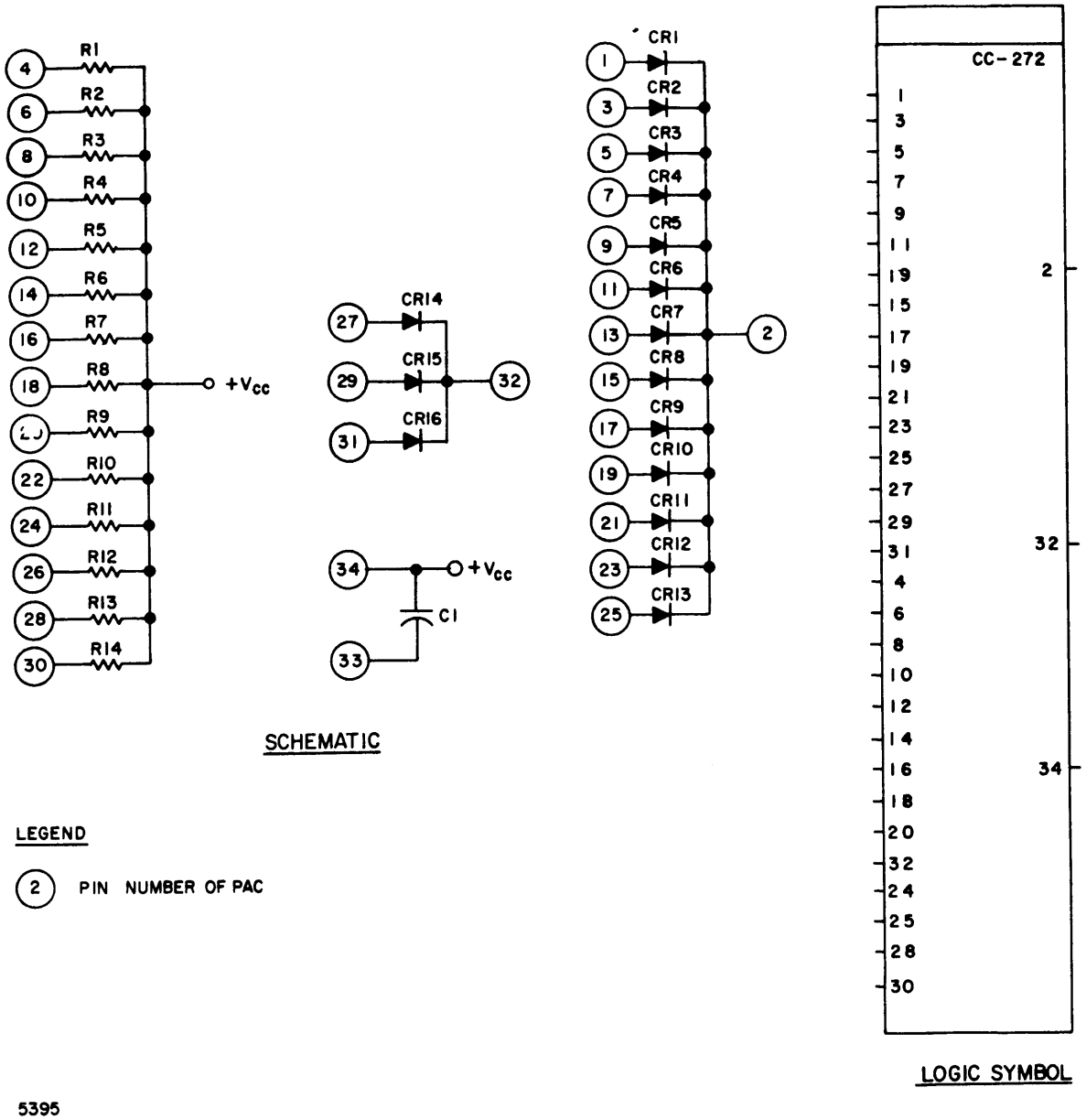


Figure CC-272-1 Diode Resistor Board Schematic

FIELD ENGINEERING MANUAL
USERS' REMARKS FORM

TITLE:

DOC. PART NO. _____

DATED _____

ERRORS NOTED:

Fold

SUGGESTIONS FOR IMPROVEMENT:

Fold

DATE _____

FROM: NAME _____

COMPANY _____ M/S _____

TITLE _____

ADDRESS _____

_____ ZIP _____

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