H316 General Purpose Digital Computer

Interface Manual

Doc. No. 70130072167A
M-495

PH

Interface Manual

H316 GENERAL PURPOSE COMPUTER

August 1969

Honeywell

Printed in U.K.

Published by the Publications Department, Honeywell Ltd., Computer Control Division.

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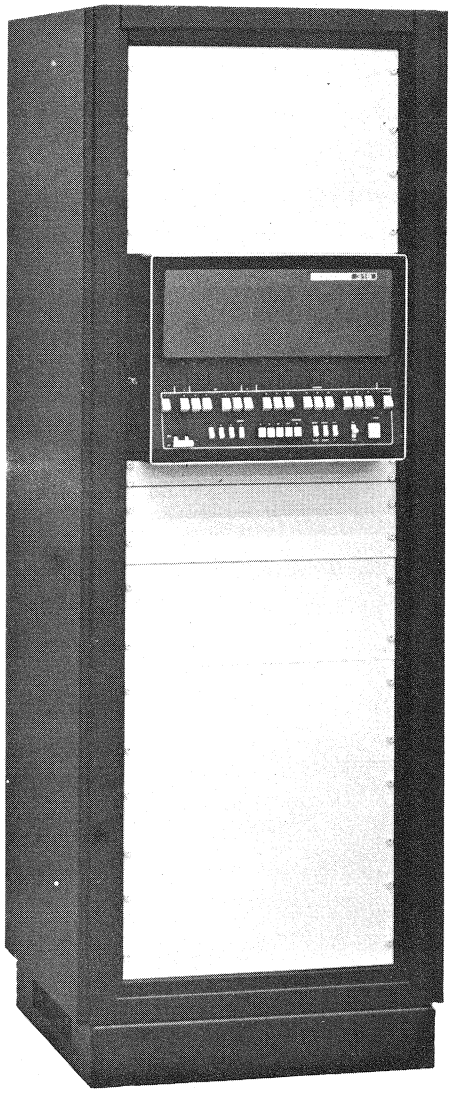


H316 General Purpose Computer

SECTION I
INTRODUCTION

SCOPE OF MANUAL

The H316 General Purpose Computer features versatile standard and optional input/output (I/O) capabilities, easy expandability through modular design, and a variety of I/O modes. This manual describes and illustrates the interface characteristics of this computer to facilitate proper connection with peripheral equipment. The basic methods of I/O transfer (standard I/O bus) and optional methods, such as the direct multiplex control option, are described in sufficient detail for system planning purposes. Data and control lines required for I/O communications are defined, timing requirements are established, and interface gating drive and load requirements are specified. Detailed descriptions of the standard and optional I/O operations of the computer are given in the Honeywell 316/516 Programmers Reference Manual.

APPLICABLE DOCUMENTS

The following documents contain information which supplements the data presented in this manual.

Title	Document No.
Honeywell 316/516 Programmers Reference Manual	42400343401
H316 Central Processor Description	42400343404
H316 Central Processor Instruction and Diagrams	70130072174

Refer to Doc. No. 42400343404 for a complete listing of the standard and optional documents which may be provided with a system.

PARALLEL I/O BUS AND OPTIONS

The standard machine, without options, communicates with peripheral equipment on a parallel I/O bus under program control. A separate instruction is required for each input or output word transfer. All peripheral devices may be tied to a single standard interrupt line (up to 20 devices may be attached). When a device requests service through the interrupt line, a programmed subroutine determines which device requires service. An optional priority interrupt system is available to eliminate the need for programmed priority determination.

The direct multiplex control (DMC) option available for use in the machine is a time-shared automatic I/O system that uses the parallel I/O bus for communication but performs

single character or block data transfers without program intervention. Two DMC models are available. The 316-20 option requires four 1.6-μs cycles for each data transfer. The H316-21 option requires four 1.6-μs cycles for the first data transfer of a block; thereafter, each transfer requires two 1.6-μs cycles. DMC transfers are interleaved with computation; the starting and terminating addresses of the memory locations to which the block of information is to be transferred are set up initially in standard memory locations under program control. The maximum transfer rate of a single standard DMC channel is one word every four cycles or 156 kHz. The maximum transfer rate of a single high-speed DMC channel is one word every two cycles or 312 kHz after the first cycle has been completed.

Each peripheral device used with the computer requires a suitable control interface compatible with the standard parallel I/O bus or the DMC option. The control interface must be capable of the following:

a. Decoding device address and function codes.

b. Providing start-stop and control signals to the device proper.

In most cases, a buffer register is required to synchronize data transfers with the machine processing cycle.

Control interfaces are provided with all optional peripheral devices available for use with this machine. The parallel channel options are standard control interfaces which may be used with special devices.

SIGNAL MNEMONICS

The electrical characteristics of the computer circuits are called: passive (+6 vdc) and active (0 vdc). The logical functions are true (logic ONE) and false (logic ZERO). In general there are two ways of relating the electrical characteristic and logical function for each signal mnemonic:

a. An assertion signal (for example, A01FF+) is logically true when it is at +6 vdc, and logically false when it is at 0 vdc.

b. A negation signal (for example, A01FF-) is logically true when it is at 0 vdc, and logically false when it is at +6 vdc.

A particular signal mnemonic can indicate assertion or negation. The sixth character of the signal mnemonic is used to specify assertion or negation. An assertion is specified by a plus sign and a negation by a minus sign. The quiescent state of an assertion signal is 0 vdc. The quiescent state of a negation signal is +6 vdc.

SECTION II
STANDARD PARALLEL I/O BUS

TRANSFER OPERATIONS

The standard computer I/O mode consists of transfers of single characters or 16-bit machine words to and from the A register of the central processor. Input transfers are performed by INA instructions, and output transfers by OTA instructions. Communication with peripheral devices is accomplished by using an I/O bus (Figure 2-1) consisting of the following:

a. Ten address lines (ADB07 through ADB16), referred to as the address bus (ADB). Least significant 6 bits specify device. Bits 7-10 specify function code.

b. Sixteen input bus (INB) input data lines (INB01 through INB16).

c. Sixteen output bus (OTB) output data lines (OTB01 through OTB16).

d. Control lines OCPLS, SMKXX, SMK01, RRLIN, CMKXX, DRLIN, PIL00, ERLXX, MSTCL, PARCK, and PWRFL.

The data processor distinguishes between devices (with respect to the destination of commands or the source or destination of data transfers) by the low order six-bit binary code of the address bus. Up to 20 devices may be paralleled on the bus.

INTERFACE CHARACTERISTICS

The control and transfer lines which make up the I/O transfer bus are described in the following paragraphs.

NOTE

Throughout the following descriptions, references are made to a "standard μ-PAC load" and to specific circuits (A, B, and C). These referenced items are fully described in the appendix of this manual.

Output Bus Lines (OTBnn+)

The 16 output data lines (twisted pair) that make up OTB are used for transmitting information from the computer's A register to the I/O device buffers. Up to 20 devices may be connected to this bus; however, each device must not load the bus with more than one μ-PAC load (see description of circuit C in the appendix).

Input Bus Lines (INBnn-)

The 16 input data lines (twisted pair) that make up the INB are used to transmit information from the I/O device buffer to the computer A register. Up to 20 devices may be

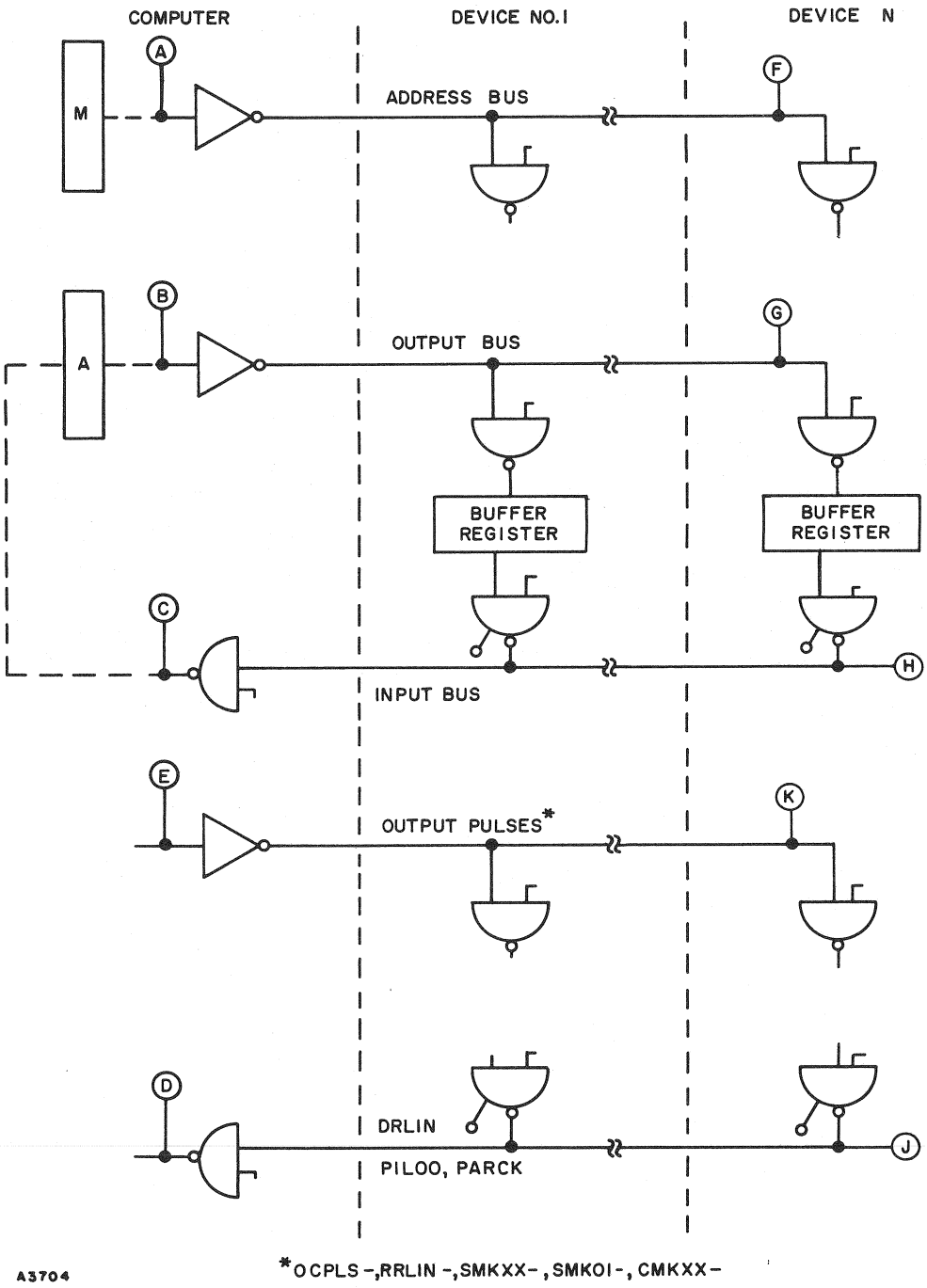


Figure 2-1. I/O Bus Functional Block Diagram

connected to this bus; however, the μ-PAC gates used to tie into the input bus must not have any collector loads (see description of circuit A in the appendix for an example of the type circuit required). The quiescent state with no information gated onto the bus is +6 vdc (logic ZERO). Each bus line is terminated at the main frame with a 500-ohm pull-up resistor. This type of termination represents four μ-PAC loads.

Address Bus Lines (ADBnn-)

The 10 address lines (twisted pair) that make up the ADB are used for addressing a device during an I/O instruction. Up to 20 devices may be connected to this bus; however, each device must not load the bus with more than one μ-PAC load. (See description of circuit C in the appendix.)

Control Line OCPLS-

Line OCPLS- is used to transmit an output control pulse to a connected device during an OCP instruction. Up to 20 devices may be connected to this bus; however, each device must not load the bus with more than one μ-PAC load. (See description of circuit C in the appendix.)

Control Line RRLIN-

Line RRLIN- carries a control pulse during an OTA instruction that is used to strobe the output bus (OTB) and to reset the ready flip-flop during OTA and INA instructions. The RRLIN- control pulse may also be used to clear the device data buffer for an INA; if used in this manner, the trailing edge of the pulse must be used to clear the buffer. Up to 20 devices may be connected to this bus; however, each device must not load the line with more than one μ-PAC load. (See description of circuit C in the appendix.)

Control Line DRLIN-

Line DRLIN- carries an input control pulse that is used by connected devices to indicate their status during an OTA, INA, or SKS instruction. Up to 20 devices may be connected to this bus; however, the μ-PAC gates used to connect the DRLIN must not have any collector loads (see description of circuit B in the appendix).

In INA and OTA transfer operations, if DRLIN becomes true before time 1740, signal RRLIN is generated and data transfer occurs. In INA and OTA transfer operations, if DRLIN becomes true between times 1740 and 2000, signal RRLIN and data transfer may or may not occur. In INA and OTA transfer operations, if DRLIN remains false through time 2000, RRLIN and data transfer do not take place. In an SKS operation, signal DRLIN must be stable and meaningful before time 1740.

NOTE

Timing diagrams for SKS, INA, and OTA operations are given in Figures 2-4, 2-5, and 2-6, respectively.

Control Line SMK01-

Line SMK01- carries an output control pulse that is used to strobe the contents of the OTB lines into device mask flip-flops during an SMK instruction. Up to 20 devices may be connected to this bus; however, only 16 devices (one per bit of the A register) are normally connected to the bus. Each device connected to SMK01- must not load the line with more than one μ-PAC load. (See description of circuit C in the appendix.)

Control Line PIL00-

Line PIL00- carries input control levels used by devices to request a program interrupt. Up to 20 devices may be connected to this line; however, the μ-PAC gates used to connect to PIL00- must not have any collector loads. (See description of circuit B in the appendix.)

Control Line CMKXX-

Line CMKXX- carries an output pulse during an SMK instruction that is used to clear device mask flip-flops. Up to 20 devices may be connected to this bus; however, only 16 devices (one per bit of the A register) are normally connected to the bus. Each device connected to CMKXX- must not load the bus with more than one μ-PAC load. (See description of circuit C in the appendix.)

Control Line PARCK-

Line PARCK- carries an input control level that is used by devices to indicate a parity fault by lighting a lamp on the system control panel. Up to 20 devices may be connected to this line. The μ-PAC gates used to connect to this bus must not have any collector loads. (See description of circuit B in the appendix.)

Control Line ERLXX-

Line ERLXX- carries an output control pulse used by the DMC option to indicate that memory end of range for the current DMC channel has been reached.

Control Line MSTCL-

Line MSTCL- carries an output control level that is used to initialize all devices connected to it.

Control Line PWRFL-

Line PWRFL- is used to carry an output control level that warns the connected devices that the computer has lost ac input power. The line originates from a relay contact in the main frame power supply. The line is normally at +6 volts. When an ac input power failure is detected, line PWRFL- goes to 0 volt approximately 1 ms before the main frame dc power fails; the line then remains at 0 until the main frame dc power is again valid.

Timing of Control Signals

The timing of the control signals carried on their respective I/O bus lines is shown in Figure 2-2. All the times shown in Figure 2-2 relate to the I/O signals at the computer (main frame) connector (points A, B, C, D and E in Figure 2-1). ("MF" in Figure 2-2 and subsequent figures means "main frame.") Data for computing the worst-case times at the farthest possible extremity of the bus (device N in Figure 2-1) follows.

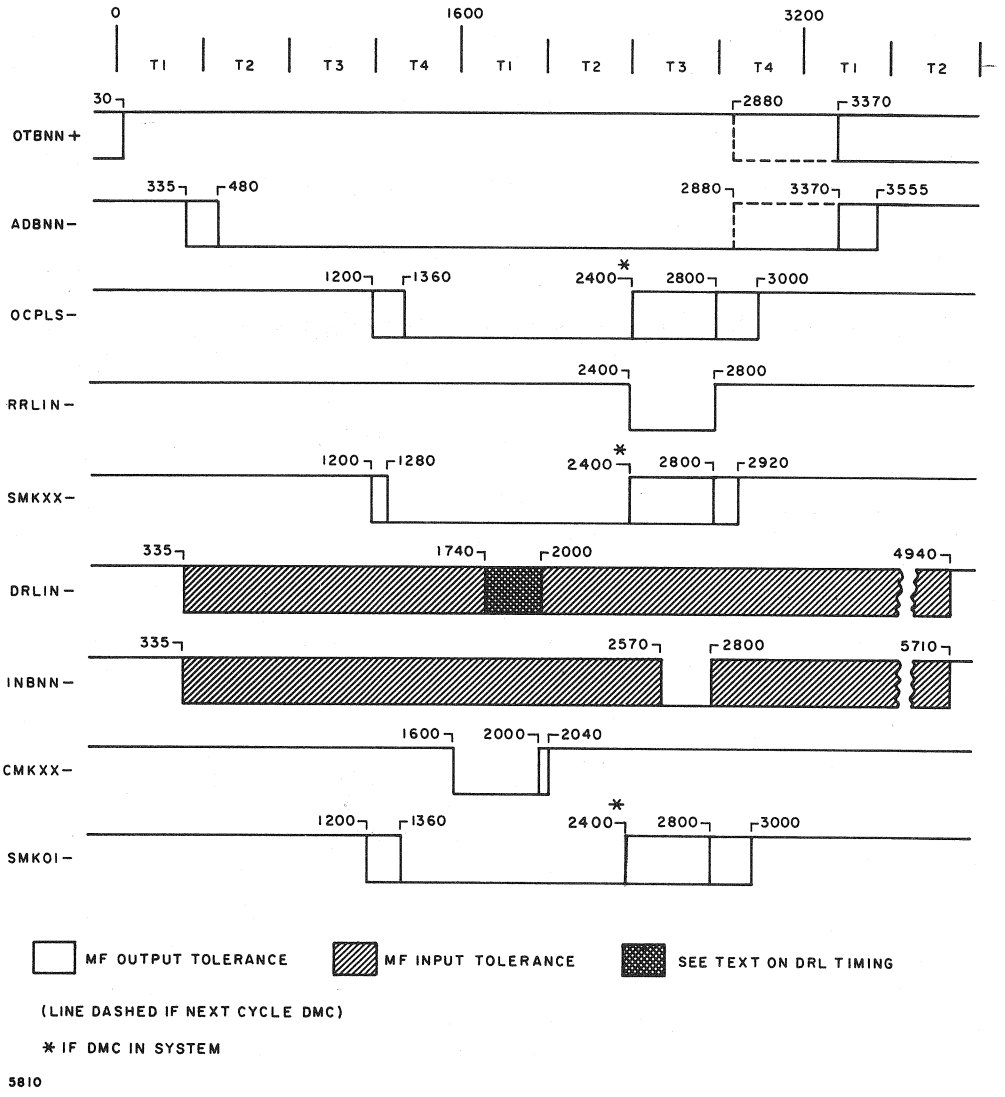


Figure 2-2. I/O Bus Control Signals, Timing Diagram

Signal	Computation of Worst-Case Times
OTBnn+	Allow 400 ns from B to G* for OTBnn+ to stabilize to the desired logic level.
ADBnn-	Allow 400 ns from A to F* for ADBnn- to stabilize to the desired logic level.
INBnn-	Allow 180 ns from H to C* for INBnn- to go positive and 155 ns from H to C* for INB to go negative.
DRLIN-	Allow 180 ns from J to D* for DRLIN- to go positive and 155 ns from J to D* for DRLIN- to go negative.
OCPLS-, RRLIN-, SMKXX-, SMK01-, CMKXX-	Allow 400 ns delay from E to K* for the output pulses. Allow 50 ns maximum for pulse width shrinkage on the bus.

*The from and to points indicated are illustrated in Figure 2-1 from the main frame circuit to or from the farthest possible device.

DEVICE COMMAND OPERATIONS

The instructions that use the I/O bus to control the operation of external devices and the manner in which the bus is used are described in the following paragraphs.

OCP Commands

OCP commands initiate motion of a device or prepare it for a specific mode of operation. No data is exchanged, and no response signal is expected from the addressed device. Only the address bus lines and the OCPLS- command pulse are involved. OCP command timing is shown in Figure 2-3.

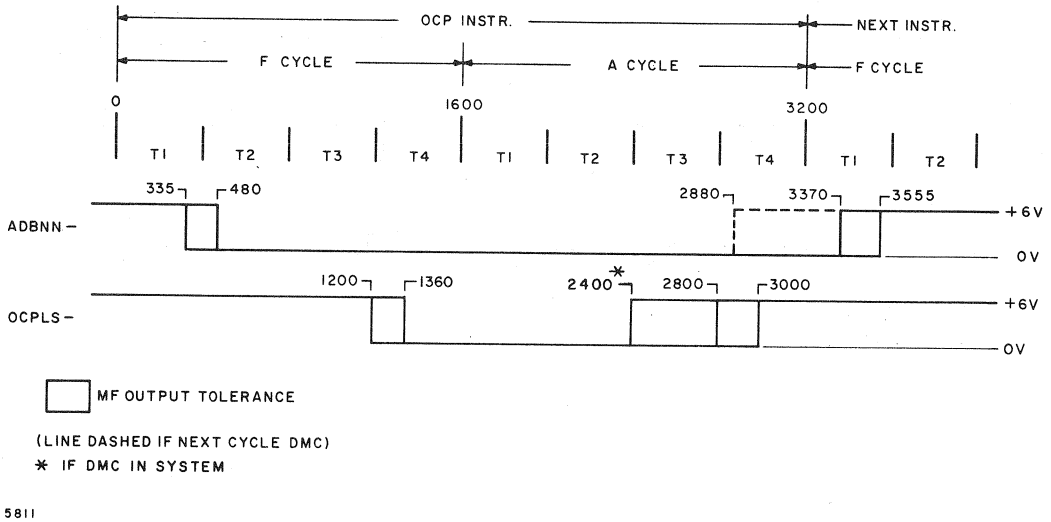


Figure 2-3. OCP I/O Command, Timing Diagram

The device address code and function code are transmitted from OCP instruction word positions 7 through 16 to the corresponding bit positions of the address bus. During the last half of the address interval, the OCPLS- command pulse occurs to enable the addressed device to perform the control function specified by the function code portion of the address. No direct response is required of the device. Any information placed by the device on DRLIN- or INB01- to INB16- is ignored by the computer during this instruction.

Typical uses of the OCP command are to:

a. Turn the high-speed paper tape punch on or off.
b. Rewind magnetic tape.

SKS Commands

The SKS command is used to test the condition of any device connected to the standard I/O bus. The command is implemented by gating the device address onto the address bus with a function code that identifies the condition being tested. If the condition is true, the device interface must bring the DRLIN- line to the 0-volt level during the time limits specified in Figure 2-4. The DRLIN signal causes a program skip of the next instruction in sequence. If the DRLIN line remains quiescent, the next instruction in sequence is executed.

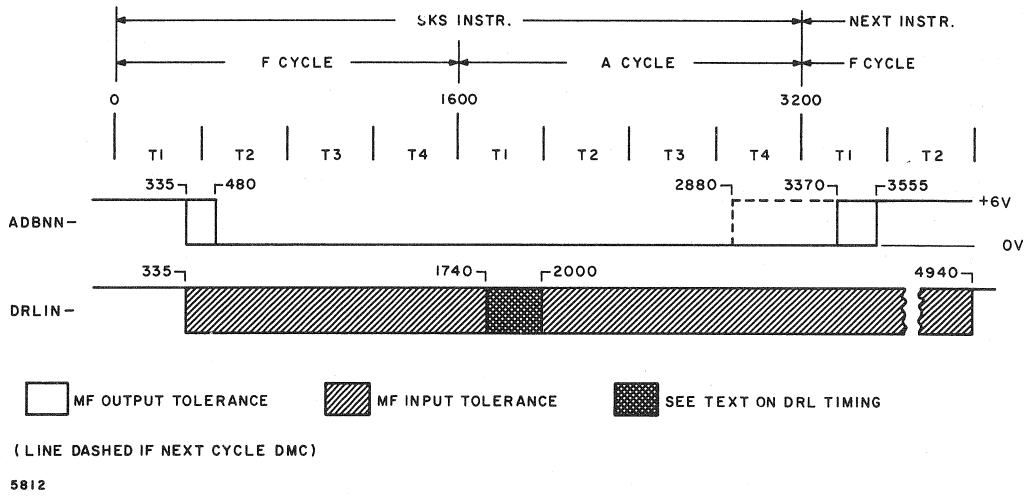


Figure 2-4. SKS Sensing Command, Timing Diagram

INA Commands

An INA command addresses a particular device and senses the device condition. If, for example, the device replies with a ready indication, the input bus is strobed to the computer A register. Timing for the performance of an INA is illustrated in Figure 2-5.

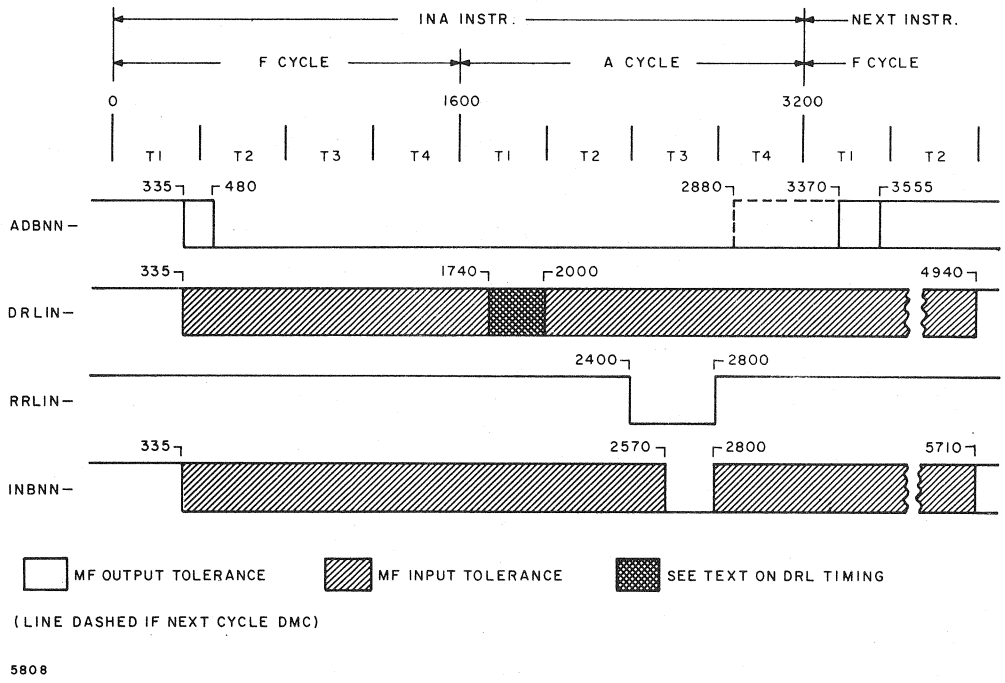


Figure 2-5. INA Input Data Transfer, Timing Diagram

INA address and function codes are placed on the address bus. The addressed device gates information onto the input bus (INB), and alerts the computer that its data is ready (DRLIN-). The timing of DRLIN is critical.

When the ready condition is detected by the CPU, data on the input bus is strobed to the A register and the next instruction is skipped. While data is being strobed into the A register, a reset ready pulse (RRLIN-) is sent out from the computer to indicate that the information has been accepted. The trailing edge of RRLIN- may be used by the device to remove the information from the input bus line (INBnn-).

OTA Commands

During an OTA output command operation, the address of the device to receive the data and output data are applied, respectively, to the address (ADB) and output bus (OTB) lines. If the device is prepared to receive the data, it sends signal DRLIN to the computer. When DRLIN is detected by the computer, it sends an RRLIN pulse to the device to strobe the data into the device buffer (the timing involved is illustrated in Figure 2-6).

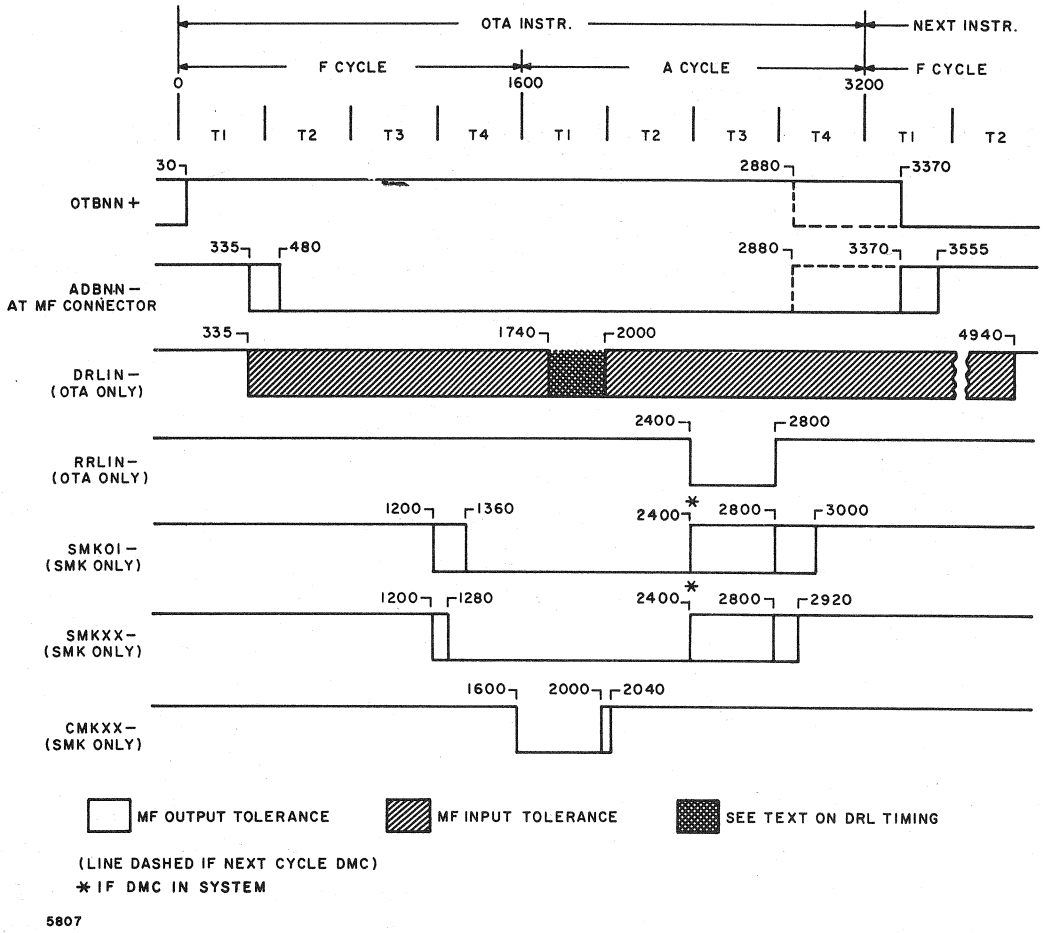


Figure 2-6. OTA Output Commands, Data Transfer Timing Diagram

SMK Commands

The SMK instruction controls, via the I/O bus, the states of mask control flip-flop circuits in each standard or optional device interface. The device address field distinguishes an SMK from an OTA instruction. Address fields that cause the computer to interpret op code 74 as an SMK are 20 and 24. All SMK instructions generate an SMKXX signal. In particular for SMK '0020, an SMK01 pulse is generated to strobe the OTB mask control bits into the respective device interface. Bit assignments for SMK '0020 are shown in Table 2-1.

Table 2-1.
Standard Interrupt Mask Assignments

OTB Bit No.	Device
1	Magnetic Tape Control Unit No. 1
2	Magnetic Tape Control Unit No. 2
3	Unassigned
4	Moving Head Disc File

Table 2-1. (Cont)
Standard Interrupt Mask Assignments

OTB Bit No.	Device
5	I/O Channel No. 1
6	I/O Channel No. 2
7	I/O Channel No. 3
8	Small Mass Store
9	Paper Tape Reader
10	Paper Tape Punch
11	ASR-33/35
12	Card Reader
13	Unassigned
14	Line Printer
15	Unassigned
16	Real Time Clock

STANDARD INTERRUPT PROVISIONS

Any system device may enable a call-for-service level line on PIL00- that diverts the computer to an interrupt subroutine. During an interrupt subroutine, SKS interrogations are performed until the busy channel is detected. The detected channel is then serviced.

The ability of standard and optional I/O devices to enable an interrupt in the computer via I/O bus line PIL00- may be inhibited (masked) selectively by the use of the set mask instruction (SMK).

PHYSICAL DESCRIPTION

The I/O bus originates in the CPU drawer (slots A1CA 20 and A1BA 20) portion of the H316 and serially connects all I/O interface logic BLOCs included in a particular system. Users desiring to interface to the H316 can, therefore, pick up the I/O bus at the last BLOC of device interface logic. No cables beyond the last interface are provided.

NOTE

The I/O bus can be connected to interfaces in the adjacent BLOC position by I/O bus jumper cable, Model 316-9101. Connection to nonadjacent BLOCs is made by μ-PAC to μ-PAC cables, Model 316-9102.

Figure 2-7 shows a typical system configuration in which two of the computer drawer assemblies are used for I/O devices. The routing of the I/O bus throughout and between the drawer assemblies is shown; all lines outside the drawer (broken lines) represent 32-conductor twisted-pair cables with μ-PAC cable connectors mounted on either end. The dotted lines within the drawer assemblies represent hard-wired lines in the device interface

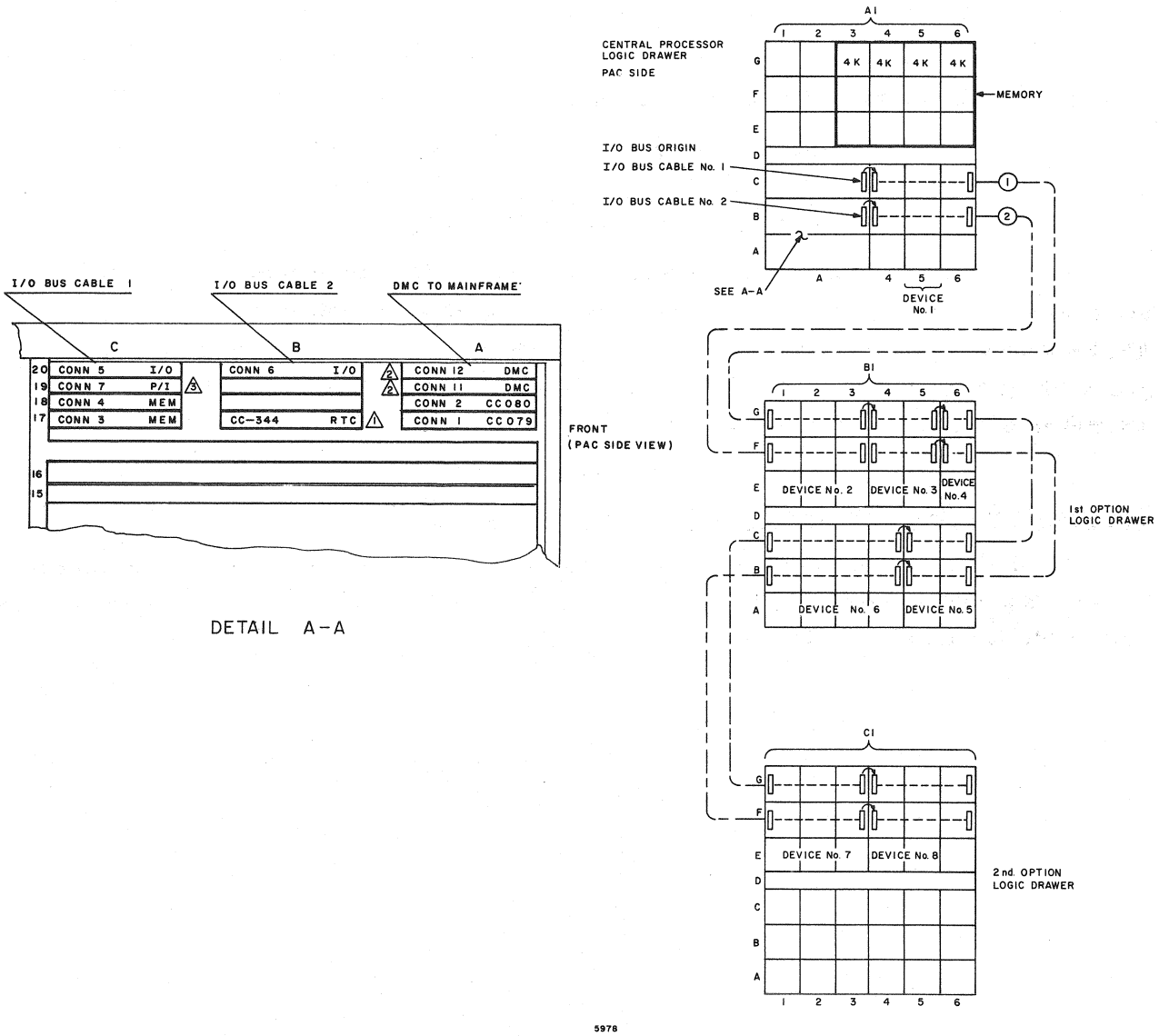


Figure 2-7. Routing of I/O Bus Through Drawer Assemblies

circuits; the curved arrows represent short 32-conductor flex cables with μ-PAC connectors mounted on both ends. The flex cables route the I/O bus lines between adjacent interface logic in the same drawer assembly; the twisted-pair cables route the I/O bus lines between the drawer assemblies.

The I/O bus has the following limitations:

a. It can drive a total of 20 options. All I/O options and some main frame options are included in the 20 option maximum. The main frame options that load the bus are:

Parallel Channels	316-32, 33, 34
Priority Interrupt	316-25
Memory Lockout	316-08
Data Multiplexed Control	316-20, 21

b. It can connect up to two drawers. The total cable length interconnecting the two drawers must not exceed 20 ft. (In addition to the standard intradrawer cabling.) The location of the interface logic for any particular system is given in documentation prepared for the specific system. The installation of equipment into the computer is described in the H316 Installation Manual.

I/O Bus Cable Signal Mnemonics and Connector Pin Assignments

As shown in Figure 2-7, two cables (No. 1 and 2) are required to carry the I/O bus transfer and control lines. The signal mnemonics and their respective pin assignments for each cable are listed in Tables 2-2 and 2-3.

Table 2-2.
I/O Bus Cable No. 1 Signal Mnemonics and Connector Pin Assignments

Pin No.	Signal	Pin No.	Signal
01	OTB01+	17	DRLIN-
02	INB01-	18	OTB06+
03	INB02-	19	OTB07+
04	ADB07-	20	INB07-
05	ADB08-	21	INB08-
06	OTB02+	22	PARCK-
07	OTB03+	23	SPARE+A
08	INB03-	24	OTB08+
09	INB04-	25	SMKXX-
10	ADB09-	26	VDC00-A
11	ADB10-	27	OCPLS-
12	OTB04+	28	VDC00-B
13	OTB05+	29	SMK01-
14	INB05-	30	VDC00-C
15	INB06-	31	ERLXX-
16	ADB11-	32	VDC00-D

Table 2-3.
I/O Bus Cable No. 2 Signal Mnemonics and Connector Pin Assignments

Pin No.	Signal	Pin No.	Signal
01	OTB09+	09	INB12-
02	INB09-	10	ADB14-
03	INB10-	11	ADB15-
04	ADB12-	12	OTB12+
05	ADB13-	13	OTB13+
06	OTB10+	14	INB13-
07	OTB11+	15	INB14-
08	INB11-	16	ADB16-
17	PIL00-	25	CMKXX-
18	OTB14+	26	VDC00-E
19	OTB15+	27	ENDOP-
20	INB15-	28	VDC00-F
21	INB16-	29	RRLIN-
22	SPARE+B	30	VDC06-A
23	PWRFL-	31	MSTCL-
24	OTB16+	32	VDC06-B

TYPICAL DEVICE CONTROL INTERFACE

A simplified logic diagram of a typical I/O device control interface is shown in Figure 2-8. The essential items are a group of address and function decoders, a ready flip-flop, a busy flip-flop, a mask flip-flop, an I/O mode flip-flop, and a data buffer. Additional logic may be added as required to accommodate special device controls or format conversion.

Standard Input Data Transfers

An SKS ready test is provided as an integral part of the INA cycle. In a device with an inherent mechanical delay between a start command and the first character delivery, the waiting period may be utilized for computation. The ready flip-flop remains reset until the device drop-in pulse (DIP) loads data into the data buffer register. If, during an INA instruction, the DRLIN line has not reached the ready condition, the computer ignores the input bus and continues with data processing. If during a subsequent test the DRLIN line indicates that the input character is ready, the data is strobed in from the input bus. Gating of data to the input bus by the decoded device address guarantees that only one device is connected to the input bus. When the ready condition permits an input transfer, the computer generates the RRLIN pulse, which resets the device ready flip-flop in preparation for another cycle. The data buffer must not be cleared until the trailing edge of RRLIN. Input transfers continue as long as the device is operating and INA instructions are executed.

Standard Output Data Transfers

During the first of a series of OTA instructions, the device buffer is cleared, its ready flip-flop is set, and the computer SKS test performed as part of the instruction is satisfied. The first data word is strobed into the data buffer by an RRLIN (OUTRRL) pulse. The device ready flip-flop is reset by the RRLIN pulse to make the device exempt from I/O transfers until the character in the device interface buffer has been taken by the device during a drop-in pulse (DIP) operation. The trailing edge of the DIP again sets the interface ready flip-flop. The I/O mode flip-flop, set to the output mode by a previous OCP, prevents data from coming into the buffer from the device; therefore DIP clears the buffer after which another word can be loaded by the next OTA cycle.

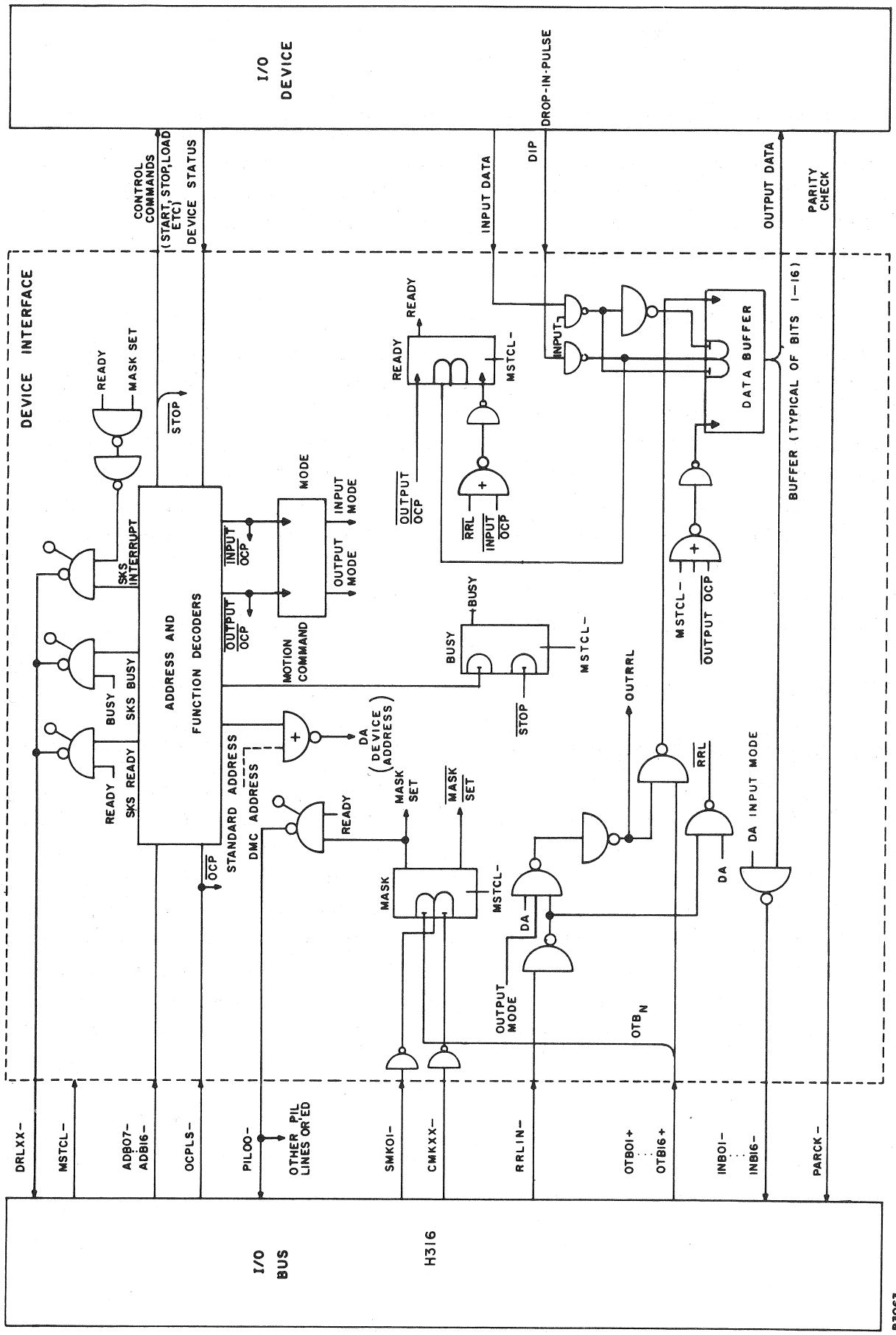


Figure 2-8. Typical Device Control Interface, Simplified Logic Diagram

Setting of Mask Flip-Flops

Mask flip-flops for all devices on the standard I/O bus are set up simultaneously by a unique instruction that gates a mask code on the output bus and produces an SMK01 pulse. Each device is assigned one output bus line; if that line contains a binary ONE, the mask flip-flop is set; otherwise, the mask flip-flop is reset. Note that the mask set instruction may be used to prevent interrupts as well as enable them.

Standard Interrupt for Output

When an OCP has enabled a device to request data from the computer, the device ready flip-flop is set concurrently and, if the mask flip-flop is set, the PIL00 line is energized. The computer immediately enters a priority subroutine in which all peripheral devices are tested by an SKS interrupt in the order of priority. An SKS interrupt command addressed to the active device is decoded and gated with MASK SET and READY. A +6v signal level on the DRLIN line permits the H316 to undergo a program jump to an OTA instruction that strobes data to the device interface buffer and resets the ready flip-flop. Removal of the ready condition deenergizes the PIL00 line. The device thus remains exempt from OTA data transfers until the drop-in pulse (DIP) takes the data and sets the ready flip-flop. The PIL00 line is again energized and another interrupt cycle is requested.

Standard Interrupt for Input

After an OCP has enabled a device to provide the computer with input data, the computer may continue with the normal program until the device drop-in pulse (DIP) delivers the first word to the interface buffer and sets the interface ready flip-flop. The ready condition, gated with the set output of the mask flip-flop, energizes the PIL00 line. The energization of the PIL00 lines forces the program to jump to a priority subroutine in which SKS interrupt instructions are addressed to the various peripheral devices in the order of priority. (Meanwhile, the interrupting device holds the data ready in the interface buffer.) An SKS interrupt command addressed to the active device is decoded and gated with MASK SET and READY. A +6v signal level on the DRLIN line permits the computer to undergo a program jump to an INA instruction that accepts the data and resets the ready flip-flop. The next drop-in pulse again sets the ready flip-flop and the cycle is repeated.

SECTION III
DIRECT MULTIPLEX CONTROL OPTION

The Direct Multiplex Control (DMC) Option, Model 316-20/21, permits high-speed I/O data transfers to be performed between the computer memory and I/O devices with a minimum of program control. Data transfers are performed via the standard OTB and INB but are controlled by the DMC rather than the central processor.

When a device in the DMC mode is ready for a data transfer, it bids for service by the DMC on a priority basis. Upon receipt of a bid, the DMC breaks into the computer program sequence and performs the data transfer between the device and the memory.

Up to 16 DMC subchannels may be controlled by the DMC unit. Figure 3-1 shows device-DMC-memory data and control flow paths.

INTERFACE

The control and data transfer lines that are required to interface the computer and DMC option are described, with the exception of OTB and INB lines, in the following paragraphs. The OTB and INB are described in Section II of this manual.

NOTE

Throughout the following descriptions, references are made to a standard μ-PAC load and to specific circuits (A, B, and C). These referenced items are fully described in the appendix of this manual.

Device Address Line (DALnn-)

This line notifies the device that it has succeeded in causing a DMC break. Each channel has one DALnn line; when a device has caused a DMC break, the DMC brings the device DALnn to ground. The quiescent state of a DALnn line is +6v. In the input mode, the signal on line DALnn must be used to gate the device buffer register to the INB. In the output mode, DALnn and RRLIN signals must strobe the OTB into the device buffer. The DALnn line must not be used to gate information onto the INB in the output mode. Circuit C (see appendix) is the type circuit used to drive each DALnn line; up to five μ-PAC unit loads may be connected to a DALnn line.

Data Interrupt Line (DILnn+)

This line receives the data transfer request from the device. Each channel has one DILnn line; the 16 lines are arranged in a priority chain. DIL line 1 (DIL01) has the highest priority; line 16 has the lowest. The DMC allows the highest priority line, among those

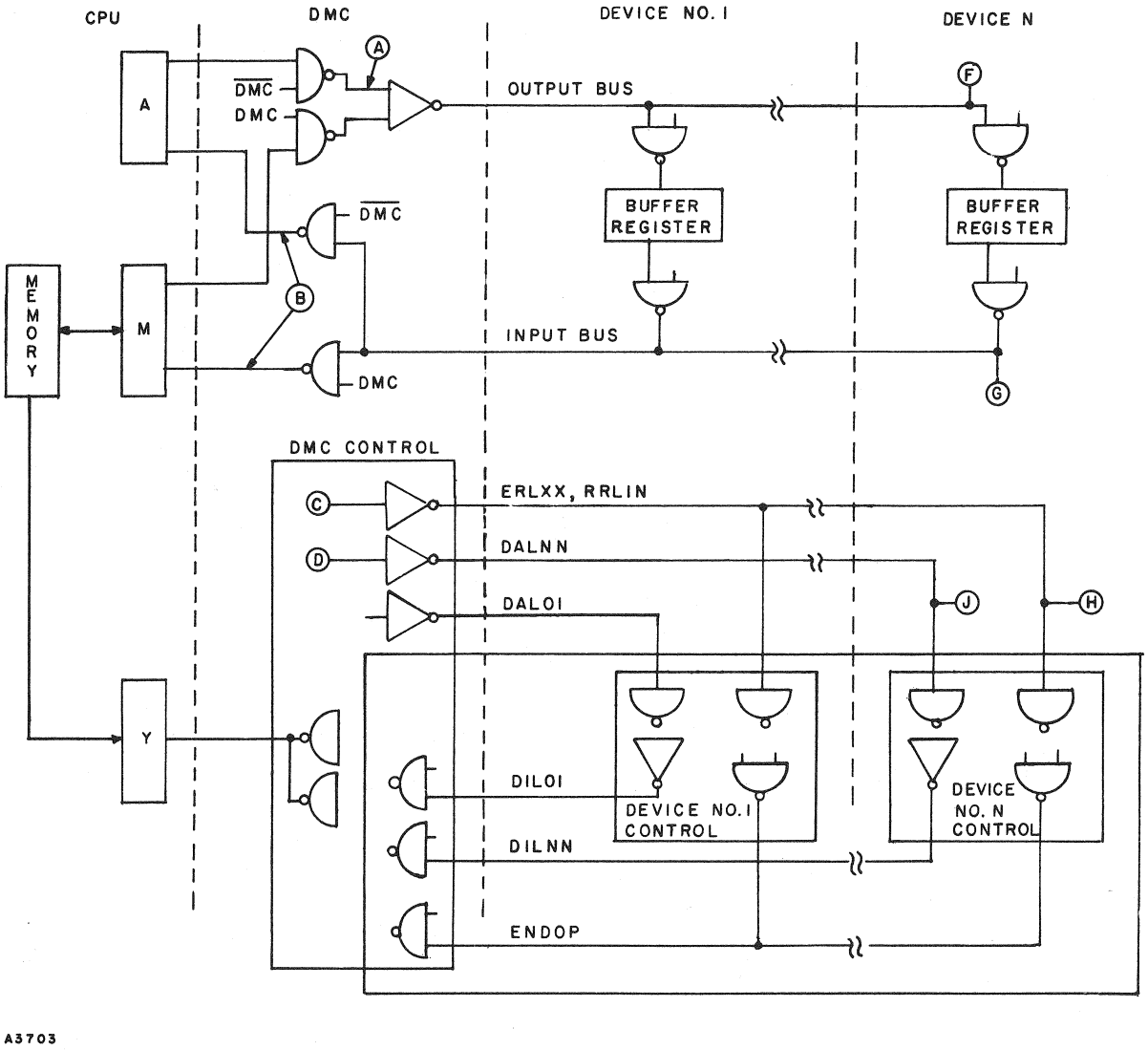


Figure 3-1. Device - DMC - Memory Data and Control Flow Diagram

requesting, to be serviced by the DMC cycle. When a device is ready to cause a DMC interrupt, it brings its DILnn to +6 volts. Each DIL must be capable of driving one μ-PAC unit load at the end of 15 feet of twisted pair.

End-of-Range Line (ERLXX-)

This line is provided to notify the device being serviced that the end of range has been reached. ERLXX is one line common to all devices. ERLXX must be gated with DAL to set a program interrupt request flip-flop. It must also disable the device from causing DIL, unless the DMC automatic subchannel switching option is being used. The quiescent

state of ERLXX+ is +6v. Each device must not load ERLXX with more than one μ-PAC unit load. Refer to the appendix for a description of the driving circuit (circuit C).

End of Operation (ENDOP-)

This line receives the end of operation signal from the device when using the high speed DMC (-21). ENDOP notifies the DMC option that the transfer operation has been terminated prior to ERL. ENDOP is one line common to all devices. Up to 16 devices may be connected to this bus. The gates used to drive ENDOP- must have no collector load (such as circuits J and K of the DI-335 PAC).

Logic levels are ground for a logic 1 and +6v for logic 0. The quiescent state of ENDOP is +6v. Upon notice from the device that transfers have terminated, the channel must generate a DIL and upon receipt of the DAL must generate ENDOP. The DIL and ENDOP must be terminated as specified on the timing diagram for the high speed DMC. No data transfer will take place on DILs accompanied by ENDOP although a normal RRL will occur. See the interface timing for ENDOP requirements.

INTERFACE TIMING

The timing of the DMC device interface is shown in Figures 3-2 and 3-3. All times shown relate to the DMC signals at the main frame, shown as A, B, C, D, and E in Figure 3-1. To compute the worst-case times at the farthest extremity of the bus:

a. OTBnn+: Allow 300 ns from A to F for OTB to stabilize to the desired logic level.

b. INBnn-: Allow 250 ns from G to B for INB to go positive and 180 ns for INB to go negative.

c. DALnn-: Allow 270 ns from D to J for DALnn to stabilize to the desired logic level.

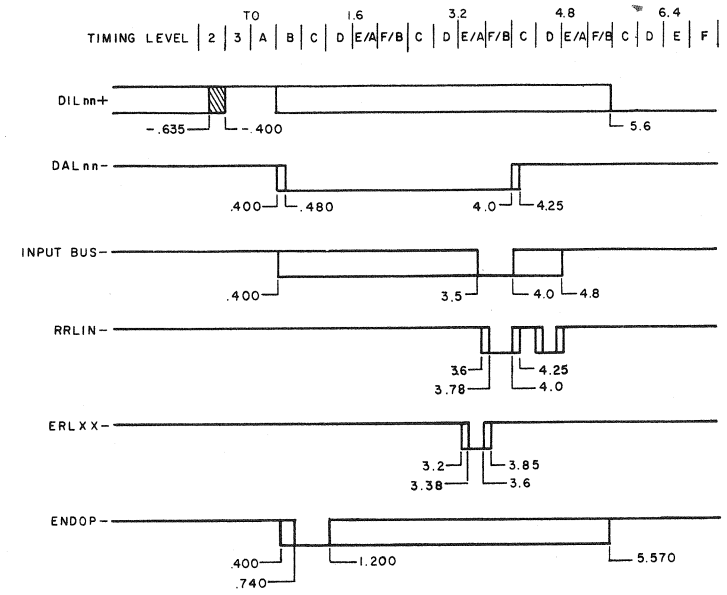
d. ERLnn-, RRLnn-: Same as DALnn

DMC INPUT MODE (See Figure 3-2.)

A particular device initiates a DMC request by bringing its DIL line to +6v. When the DMC is ready to service this request, it brings the DAL of this device to 0v. All the times shown on Figures 3-2 and 3-3 are referenced to the starting of the DMC Timing Level Generator (TLG).

The device uses DAL to gate the contents of its buffer onto the INB. INB must be stable and meaningful at the main frame connector, 3.1 μs for the standard DMC and the first transfer of the high-speed DMC, from the time DAL goes to ground (0v) and 1.3 μs for the high-speed transfer other than the first from the time DAL goes to ground (0v). INB must remain stable and meaningful for 0.5 μs.

The trailing edge of RRLIN signifies completion of the data transfer, and can be used to reset the buffer register. RRLIN should also be used to reset ready and remove the DMC request. The DMC request (DIL) must be removed by 5.12 μs for the standard DMC and the

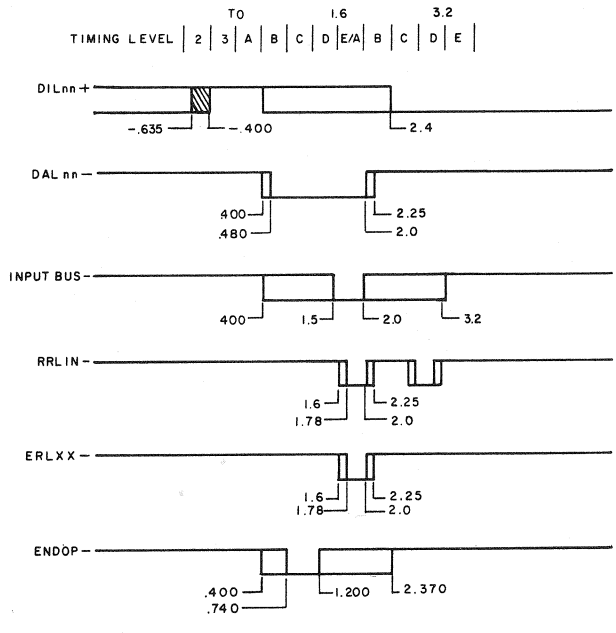


NOTE: TIMING LEVEL F ONLY USED IN STANDARD DMC
ENDOP- ONLY USED IN HIGH-SPEED DMC

DIL MAY OR MAY NOT CAUSE A DMC CYCLE
ALL TIMING IN MICROSECONDS.

STANDARD DMC AND FIRST CYCLE OF HIGH-SPEED DMC

6110

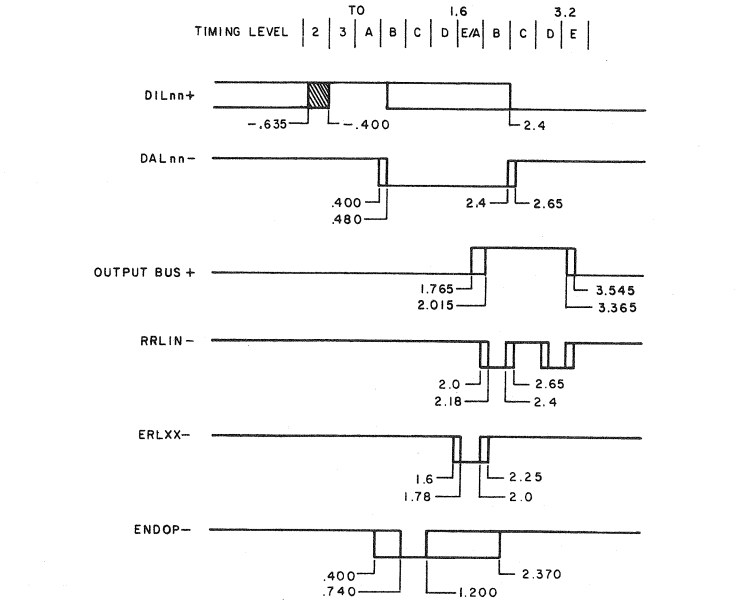


DIL MAY OR MAY NOT CAUSE A DMC CYCLE.
ALL TIMING IN MICROSECONDS

OTHER THAN FIRST CYCLE OF HIGH-SPEED DMC.

6111

Figure 3-2. DMC Interface - Input Mode



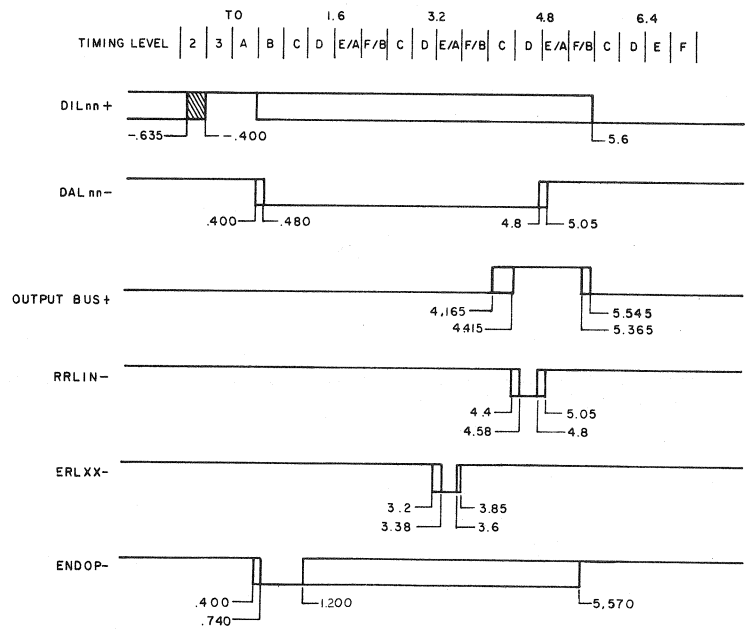


Figure 3-3. DMC Interface - Output Mode

first transfer of the high-speed DMC and 1.92 μs for all other transfers after DAL goes to 0v. It can be seen from Figure 3-2 that a second RRLIN occurs. This is redundant and can be ignored since it occurs after DAL has been removed.

DMC OUTPUT MODE (See Figure 3-3.)

A particular device initiates a DMC request by bringing its DIL line to +6v. When the DMC is ready to service this request, it brings the DAL of this device to 0v.

When the DMC has loaded the output bus with the data to be transferred, it generates RRLIN to be used to strobe the OTB into the device buffer.

There is one restriction on the method used to gate OTB into the device buffer. A device must not use the leading edge of RRL to gate the inverted OTBnn+ into the 0 side of the buffer register which has been previously cleared to ONEs. RRLIN should also be used to remove the DMC request. The DMC request (DIL) must be removed by 5.12 μs for the standard DMC and the first transfer of the high-speed DMC and 1.92 μs for all other transfers after DAL goes to 0v. It can be seen from Figure 3-3 that a second RRLIN occurs on transfers other than the first on the high-speed DMC. This is redundant and can be ignored since it occurs after DAL has been removed.

DMC SUBCHANNEL

The DMC control unit is connected to a device through a DMC subchannel. The DMC subchannel contains the necessary logic to permit the device to operate in the DMC mode. It is available on many standard I/O devices.

Physical Description

A device operating under DMC control has its interface connected to the standard I/O bus. The interface is modified by the inclusion of both additional logic (called a "DMC subchannel") and a cable connection to the DMC control unit (cable no. 3). The standard I/O bus cables are connected to the interface in the normal I/O fashion (Figure 3-4). The DMC cables (Table 3-1) connect the DIL and DAL lines to the device interfaces.

If two or more devices in a drawer operate under DMC control, the DIL/DAL lines are hard-wired from one interface to the next. (See Figure 3-4.) If a second drawer contains DMC device interfaces, a second DIL/DAL cable (cable no. 4) is provided. DMC device interfaces should not be placed in more than two drawers.

Figure 3-4 shows a typical system configuration using standard I/O devices and DMC devices. All lines shown outside the drawers are 32-conductor twisted-pair cables with cable PACs mounted on either end (model 316-9102). The dotted lines within the drawer assemblies represent wires which are wire-wrapped in the device interface. The curved arrows represent 32-conductor flex cables with cable PACs mounted on both ends (model 316-9101).

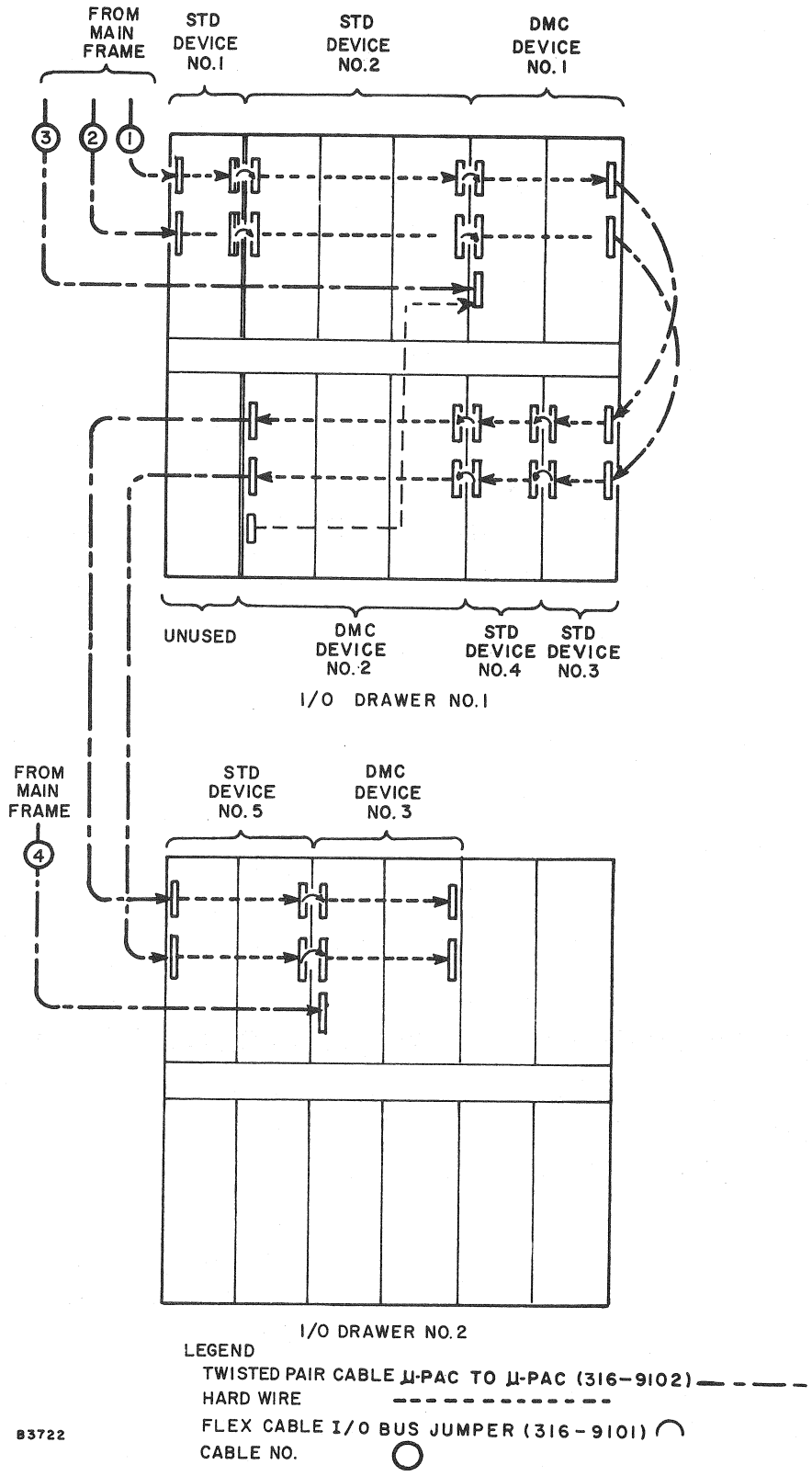


Figure 3-4. Standard Devices

Signal Placement

Cable No. 1 Same as standard I/O bus
Cable No. 2 Same as standard I/O bus
Cable No. 3 See Table 3-1
Cable No. 4 See Table 3-1 (same as cable no. 3)

Table 3-1.
DMC Cable No. 3, Signal Mnemonics and Connector Pin Assignments

Pin	Signal Name	Pin	Signal Name
01	DIL01+	02	DAL01-
03	DIL02+	04	DAL02-
05	DIL03+	06	DAL03-
07	DIL04+	08	DAL04-
09	DIL05+	10	DAL05-
11	DIL06+	12	DAL06-
13	DIL07+	14	DAL07-
15	DIL08+	16	DAL08-
17	DIL09+	18	DAL09-
19	DIL10+	20	DAL10-
21	DIL11+	22	DAL11-
23	DIL12+	24	DAL12-
25	DIL13+	26	DAL13-
27	DIL14+	28	DAL14-
29	DIL15+	30	DAL15-
31	DIL16+	32	DAL16-

Typical DMC Subchannel

Standard I/O device interfaces may be optionally provided with subchannel logic for operation under DMC control. The required additional logic consists of a DMC enable control logic to produce the DILnn device bid to DMC signal. A simplified diagram of the required logic is shown in Figure 3-5.

In DMC operation, the DMC address (DAL) is used in lieu of the standard address to prepare the interface for either an input or output data transfer. The DMC enable flip-flop circuit is set by a special DMC mode OCP command and in turn enables the associated DILnn output line.

The receipt of an end-of-range (ERL) signal from the DMC option causes the DMC ready control flip-flop to be reset, thus inhibiting the generation of further DILnn outputs to the DMC option until the control flip-flop is again set by a programmed OCP instruction.

With the exception of the control provisions described, DMC subchannel data transfers occur in the same manner and use the same I/O and control lines as the computer I/O bus.

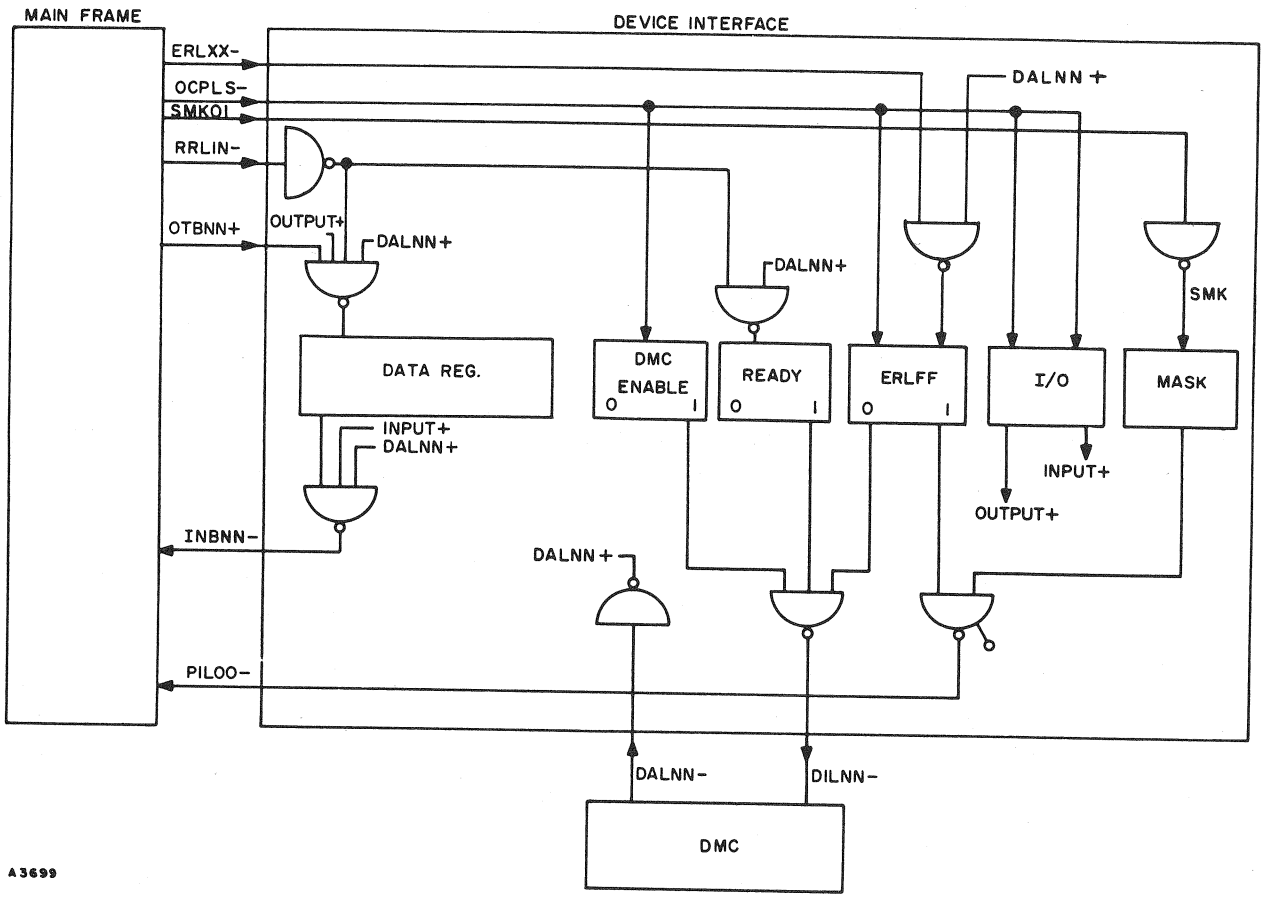


Figure 3-5. Typical DMC Subchannel Device Interface

SECTION IV
PRIORITY INTERRUPT OPTION

The Priority Interrupt (PI) Option, Model 316-25, expands the capability of the standard system interrupt provisions by enabling the addition of up to 48 interrupt control lines to the system which operate via a priority network in the option. Each of the possible 48 optional interrupt lines is assigned a specific priority level in the option and a unique memory location in the computer memory (see Table 4-1).

In addition to the priority control network, the PI option provides a means of storing each interrupt bid until it is serviced and control logic which permits the interrupt lines to be masked (inhibited) selectively under program control.

INTERFACE

All data transfer, mask, and address operations performed between the central processor and the interface of a device requesting service via the PI option are accomplished through the standard I/O bus OTB, INB, and ADB lines (see Section II).

Table 4-1.
PI Interrupt Lines, Assigned Memory Locations

PI Line	Dedicated Address	PI Line	Dedicated Address
01	00064	25	00114
02	00065	26	00115
03	00066	27	00116
04	00067	28	00117
05	00070	29	00120
06	00071	30	00121
07	00072	31	00122
08	00073	32	00123
09	00074	33	00124
10	00075	34	00125
11	00076	35	00126
12	00077	36	00127
13	00100	37	00130
14	00101	38	00131
15	00102	39	00132
16	00103	40	00133
17	00104	41	00134
18	00105	42	00135
19	00106	43	00136
20	00107	44	00137
21	00110	45	00140
22	00111	46	00141
23	00112	47	00142
24	00113	48	00143

Interrupt Line Signal Requirements

The circuitry controlling each priority interrupt input line must be capable of driving one μ-PAC load at the end of the required interconnecting cable (refer to the appendix for a definition of a standard μ-PAC load). Each PIL line can generate an interrupt request by using any of the following:

a. A positive-going pulse (ground to +6v) with a minimum duration of 40 ns (trailing edge used).

b. A negative-going pulse (+6v to ground) with a minimum duration of 60 ns (leading edge used).

c. A negative-going step function from +6v to ground.

The timing of the external device interrupt request pulse is not critical; the option detects and stores each input request until the request is serviced or the option is cleared.

PI Interrupt

A simplified functional diagram illustrating the use of the PI option by peripheral devices is shown in Figure 4-1. As shown, device interrupt request lines to PI (PIL01-PIL48) are connected to a priority circuit via mask logic. During each TL2 clock period, the computer transmits a sampling pulse to the PI option that gates to the computer a priority interrupt request signal (PIREQ) and the channel address code of the enabled input line with the highest priority.

The PI mask logic is controlled by inputs from the standard I/O bus lines (OTB, ADB, and SMKXX) (see Section II). In addition to being controlled by the mask, PI interrupt requests (PIREQ) to the computer may also be blocked by an inhibit interrupt (INH) instruction.

OPTIONAL EQUIPMENT

A memory increment (MI) option, Model 316-26, may be added to a PI option to enable the PI optional interrupt lines to be converted, in groups of four, to memory increment lines. MI requests are handled by the PI option in the same manner as the PI requests. When selected, however, MI requests cause a 1 to be added to the contents of the memory location assigned to the converted PI optional interrupt line.

The memory increment action is not subject to inhibition by the INH instruction (central processor permit interrupt control flip-flop).

Conversion of PI Lines

Any number of groups of four operational interrupt lines may be converted to MI lines; however, the groups converted must be consecutive, starting with the basic group (PI lines 1 through 4). Since the conversion to MI lines must start with the basic group of PI lines, MI always has higher priority than other PI lines.

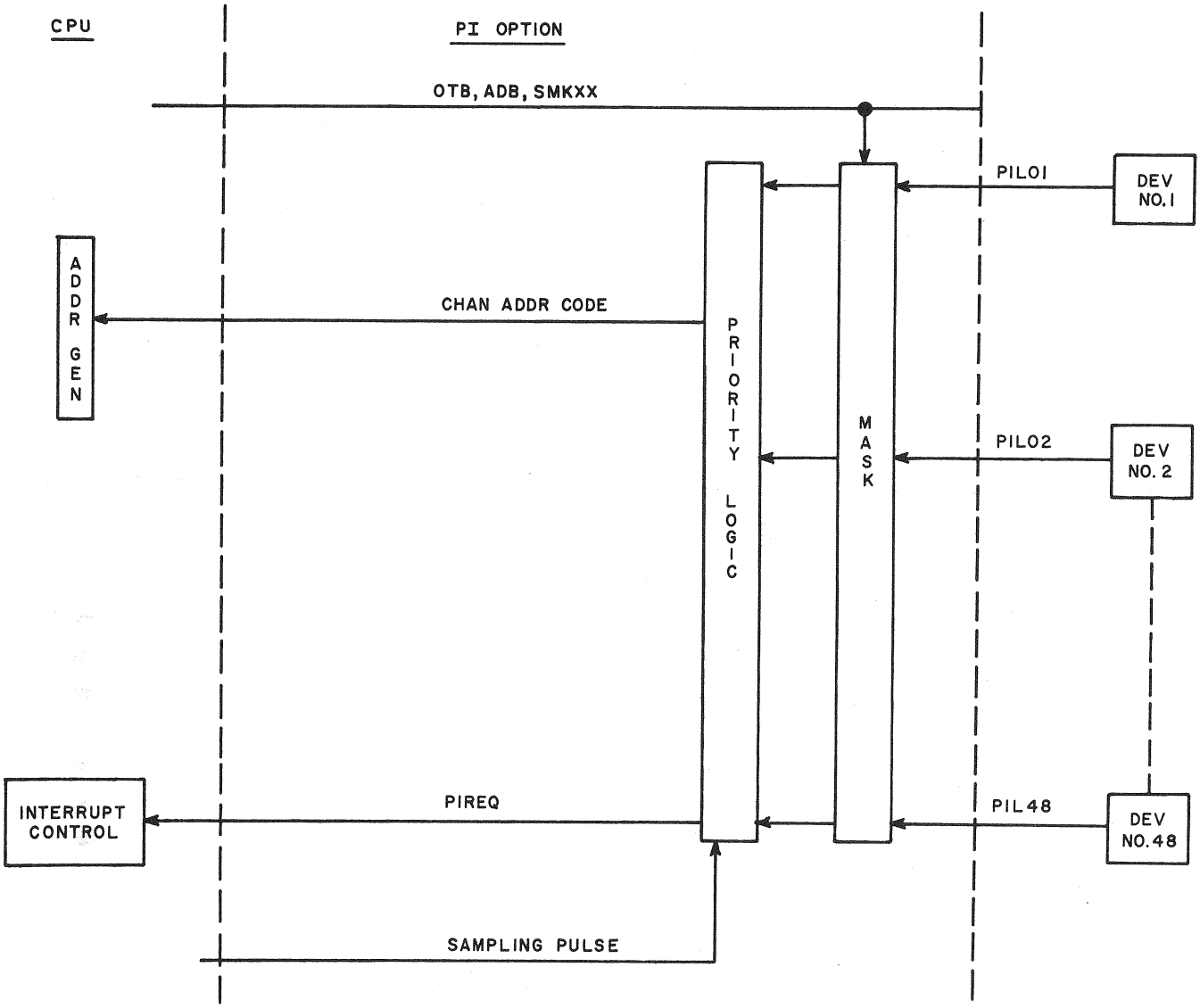


Figure 4-1. PI Requests, Option/CPU Block Diagram

MI

A simplified functional diagram illustrating the use of MI lines by peripheral devices is shown in Figure 4-2. As shown these lines request a break in the same manner as the standard priority interrupt lines; however, whenever a channel address code of an MI line is gated from the option, it is accompanied by a single execute request signal (SEXRQ) as well as the PIREQ signal.

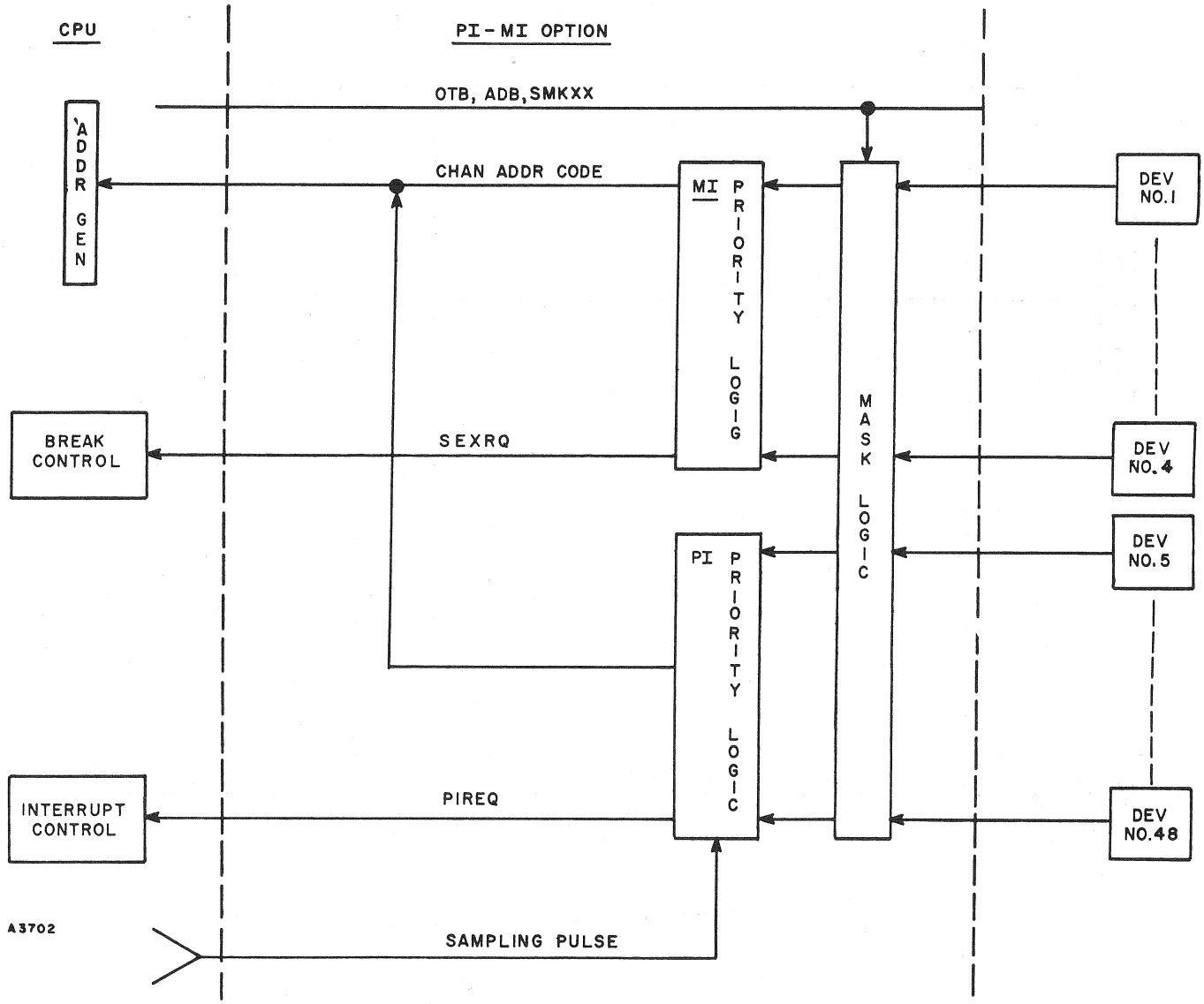


Figure 4-2. MI Requests, Option/CPU Block Diagram

PHYSICAL DESCRIPTION

The placement of a PI option in a typical system I/O drawer assembly is illustrated in Figure 4-3. As shown in A of Figure 4-3, when more than 16 channels are required, the customer is provided with up to three option/device interconnecting cables (cables 1, 2 and 3 of Figure 4-3). Each cable is a standard 32-conductor (twisted pair) μ-PAC cable; the mnemonic and pin assignment of each signal carried in the three interconnecting cables are listed in Table 4-2. When 16 or fewer PI channels are required in a system, only one interconnecting cable is required (see B of Figure 4-3).

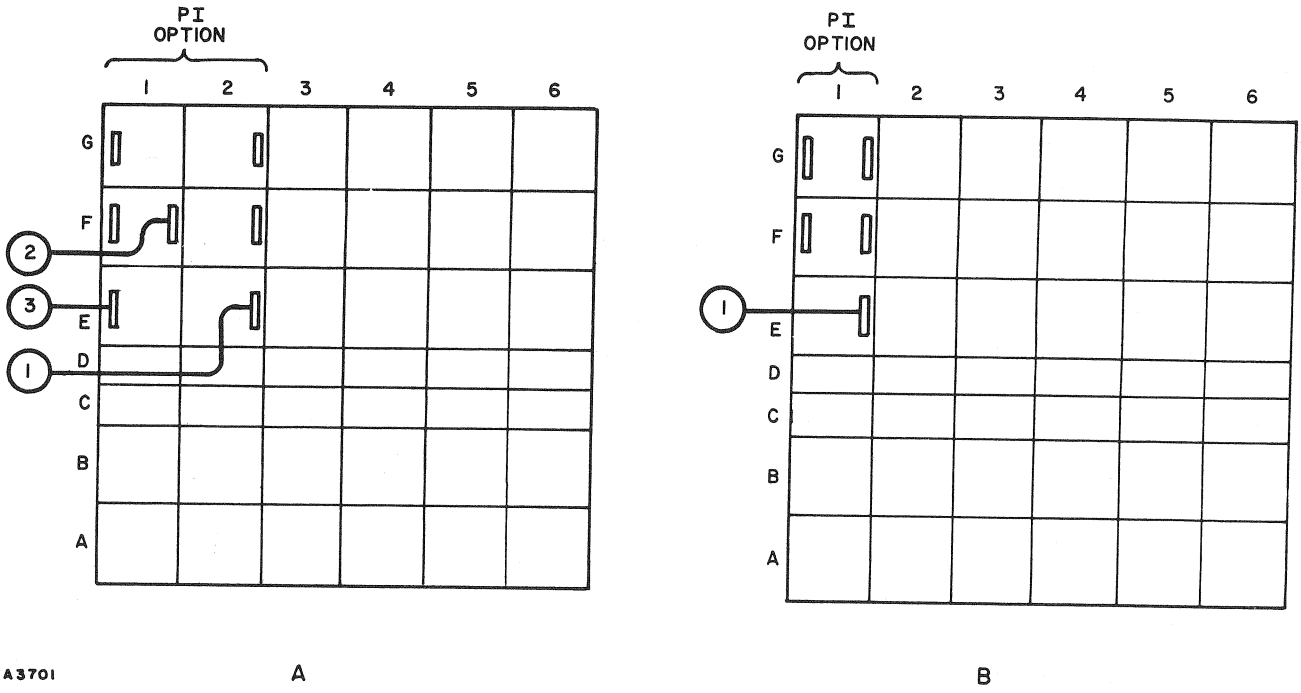


Figure 4-3. Standard Device Logic BLOC Layout

Table 4-2.
Priority Interrupt Cables,
Signal Mnemonics and Connector Pin Assignments

Cable Connector Pin No.	Signal Mnemonics		
	Cable No. 1	Cable No. 2	Cable No. 3
1	PIL01	PIL17	PIL33
3	PIL02	PIL18	PIL34
5	PIL03	PIL19	PIL35
7	PIL04	PIL20	PIL36
9	PIL05	PIL21	PIL37
11	PIL06	PIL22	PIL38
13	PIL07	PIL23	PIL39
15	PIL08	PIL24	PIL40
17	PIL09	PIL25	PIL41
19	PIL10	PIL26	PIL42
21	PIL11	PIL27	PIL43
23	PIL12	PIL28	PIL44
25	PIL13	PIL29	PIL45
27	PIL14	PIL30	PIL46
29	PIL15	PIL31	PIL47
31	PIL16	PIL32	PIL48

APPENDIX
CIRCUITS

UNIT LOAD DEFINITION

Loading specifications for μ-PACs are expressed in terms of "unit loads" both for input loading and output drive capability. The unit load concept simplifies calculation of total loading imposed in a driving stage that is fanned out to a number of different circuit types. For μ-PACs, a unit load is defined as the power required to drive the input circuit of a NAND gate (nominally 1.6 ma with a maximum of 2.0 ma). Unit load ratings apply to the active (ground) signal condition at a gate input. A load requires no input power when the input is passive (+6vdc).

CIRCUIT DESCRIPTIONS

Descriptions of the circuits (designated A, B, C, and D for reference purposes) required to drive computer data and control input lines and to terminate or load computer output lines are presented in the following paragraphs.

Circuit A, Input Bus (INB) Circuits

As illustrated in Figure A-1, the driving source for a type A circuit is a saturated transistor with the emitter connected to ground. The specified voltage for the active level is 0 to 0.35 volt maximum. The driving source is an open circuit for passive levels. Equivalent driving circuits must have the characteristics described. The following μ-PAC circuits or their equivalents may be used to drive INB lines as shown in circuit A.

Circuit	μ-PAC
J, K	CC-151
A thru P	CC-152

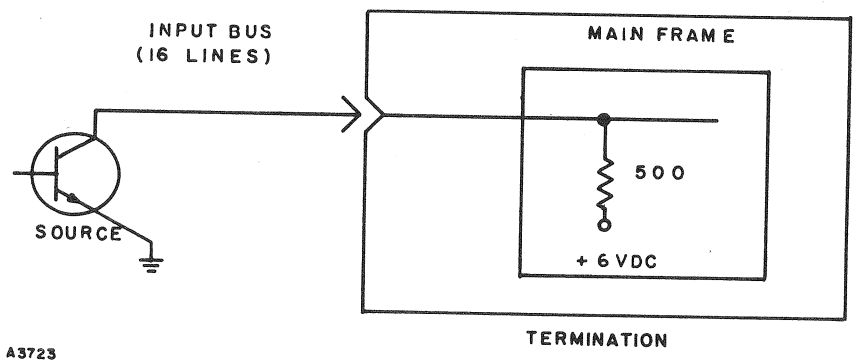


Figure A-1. Circuit A

Circuit B, Input Control Signal Driving Source

As illustrated in Figure A-2, the driving source for circuit B is similar to that of circuit A; the only difference between the two is that circuit B is terminated as shown, and circuit A is terminated in a 500-ohm resistor.

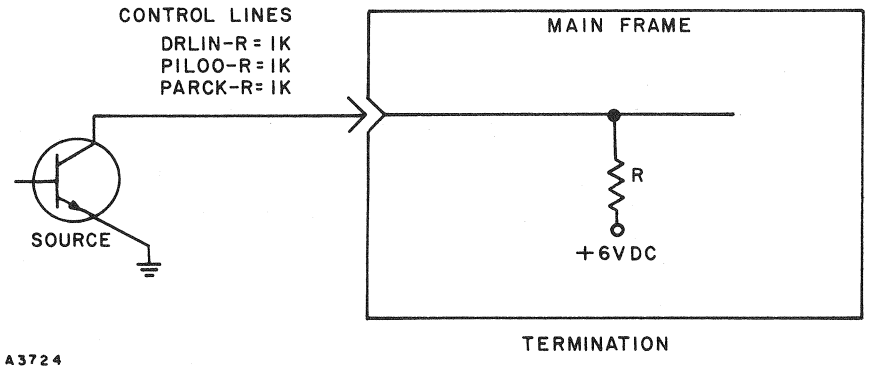
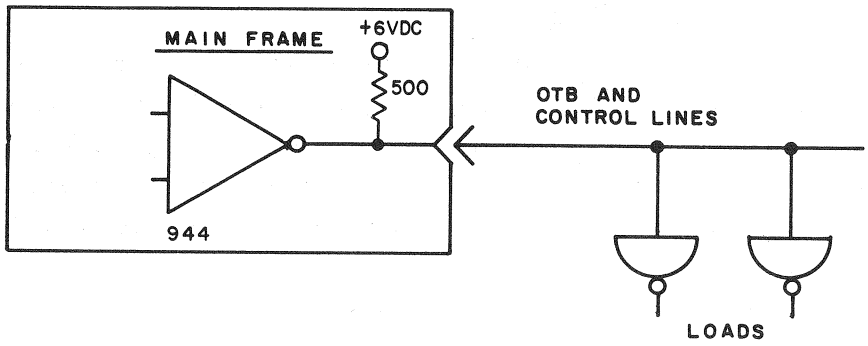


Figure A-2. Circuit B

Circuit C, Output Bus (OTB) and Control Signal Line Loading Circuits

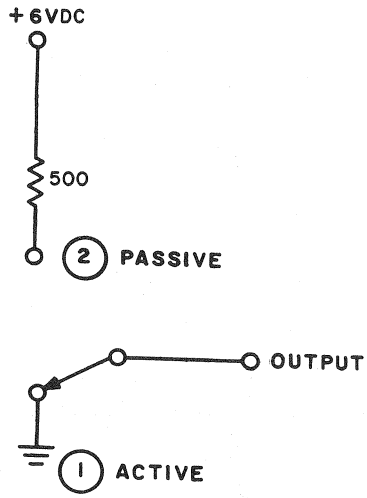
Figure A-3 illustrates the manner in which a computer output line is loaded and shows an equivalent circuit for line source impedance. Each output line amplifier is capable of supplying up to 36 ma of current to a positive supply when its output is in the active state (0 to 0.50 vdc). The output circuit is not designed to sink or supply dc current when the output is in the passive state (+4.0 to +6.3 vdc). All loads should disconnect when the inputs are more than +2.5 vdc.

Typical line output impedance characteristics are indicated in the equivalent circuit of Figure A-3. As shown, when switching from an active to a passive state, the circuit goes from position 1 to 2.

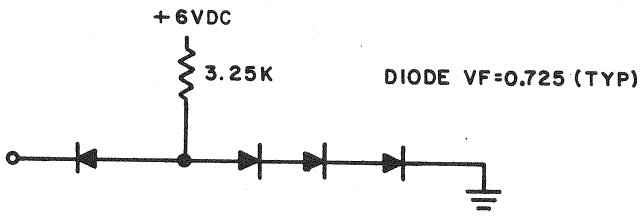


A

CIRCUIT C



B



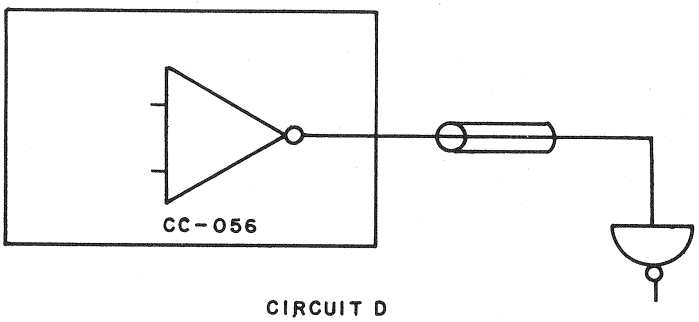
C

LOAD IMPEDANCE

Figure A-3. Circuit C, Typical Circuit and Equivalent Source and Load Impedances

Circuit D, Output Signals from Parallel Channels

Figure A-4 illustrates a line driver that is capable of driving up to 50 feet of 62-ohm twisted-pair wire. The line driver is designed to drive one unit load. In the passive state the output voltage is +4.5 ±0.5 vdc. In the active state the output voltage is 0 to 0.35v. The circuit is protected against accidental grounding of the output via the 62-ohm current limiting resistor in series with the output. The load circuit should disconnect when its input is passive (+4.5 vdc).



CIRCUIT D

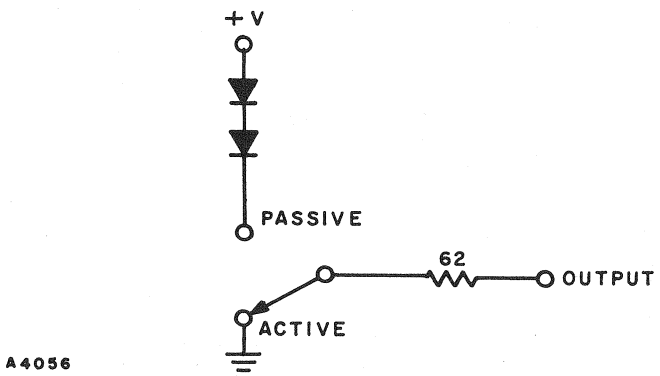


Figure A-4. Circuit D

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