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DDP-516-20
DATA
MULTIPLEXED CONTROL

Option Manual

May 1968

Honeywell

COMPUTER CONTROL DIVISION

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NOTE

This manual includes changes in accordance with the following ECOs: 3941, 4477, 5092 and 5285

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ILLUSTRATIONS

DDP-516-20
DATA MULTIPLEXED CONTROL

INTRODUCTION

The data multiplexed control (DMC) option provides direct access for input/output data transfers between the memory of the DDP-516 General Purpose Computer and external devices requiring this service.

Multiplexed service provides either 4, 8, 12, or 16 channels, each being serviced according to its priority. Channel 1 has the highest priority and channel 16 the lowest.

A maximum data transfer rate of one word every 3.84 μsec can be attained when only one channel is being used.

Reference Documents

Instruction Manual for DDP-516 General Purpose Computer: Volume I, Doc. No. 130071620; Volume II, Doc. No. 130071621; Volume III, Doc. No. 130071622.

Interface Manual for DDP-516 General Purpose Computer, Doc. No. 130071624.

Physical Characteristics

The DMC option consists of integrated μ-PACs packaged in a 1 x 3 BLOC and inserted into DDP-516 main frame.

Functional Description

The function of the DMC is to control the execution of data transfers between the memory and the devices using one of the 16 DMC channels via the standard I/O bus. Each channel is assigned two consecutive memory locations. The starting address for the data transfer is stored in the first location; the terminal address is stored in the second.

When a device has data for the memory or requires data from the memory, the device uses the DMC control lines to request service. (See Figure 1.) The DMC then generates a break request to the CPU. After the CPU has completed the current instruction, a DMC cycle is executed. During this cycle the appropriate transfer between the external device and the computer memory takes place using the standard I/O bus of the DDP-516 main frame.

OPERATION

Instructions for operating the various DMC devices can be found in operation instructions for that particular unit.

Preliminary programming necessary for operating a device is:

a. Store starting address in the assigned location, with bit 1 a ONE for input mode or ZERO for output mode. See Table 1.

b. Store terminal address in assigned location. See Table 1.

c. If a program interrupt is desired when end-of-range is reached, the PI mask flip-flop for the device must be set to a ONE and the desired interrupt routine must be part of the program.

d. Using appropriate OCPs, set up device in input or output mode and then set device to DMC mode. The order of these OCPs is specified in each device specification.

Table 1
Starting and Final Address Locations

Channel	Starting Address	Final Address
1	20	21
2	22	23
3	24	25
4	26	27
5	30	31
6	32	33
7	34	35
8	36	37
9	40	41
10	42	43
11	44	45
12	46	47
13	50	51
14	52	53
15	54	55
16	56	57

INSTALLATION

PAC Locations

The DMC option consists of integrated μ-PACs located in a 1 x 3 BLOC inserted in the DDP-516 main frame.

Four additional μ-PACs listed below are required in the main frame.

μ-PAC	Slot Location
PA-336	A1 B26
TG-335	A1 C26
TG-335	A1 B25
CM-022	A1 D52

Removal of μ-PAC CC-054 at location A1 C42 is necessary.

Power Source

The DMC unit power requirements are supplied by the main frame (+6v) power supply.

Interface Connections

Connections between the I/O bus and interface logic are shown on LBD 224 for the DMC. For further information refer to 3C Doc. No. 130071624 (Interface Manual for DDP-516 General Purpose Computer).

THEORY OF OPERATION

Refer to Table 2 for a description of DMC mnemonics. See Figure 1 for DMC signal interface block diagram, and LBD 220 through 224 for DMC logic.

Table 2
Function Index

Mnemonic	Description
ADREN	Address Enable to IY Bus
CO14X	Carry out from any of channels 1 through 4
CO18X	Carry out from any of channels 1 through 8
CO112	Carry out from any of channels 1 through 12
CO116	Carry out from any of channels 1 through 16
DALEN	Device Address Line Enable
DALnn	Device Address Line, Channels 1-16
DCRnn	Address Counter Register Bit nn
DCY2X	DMC Cycle, Phase 2
DCY3X	DMC Cycle, Phase 3
DCYXX	DMC Cycle
DILnn	Data Interrupt Line, Channels 1-16
DMC1X	DMC Cycle, Phases 1 and 2
DMC2X	DMC Cycle, Phases 2 and 3
DMCRQ	DMC Request
DMCRR	DMC Reset Ready Line
DMCWR	DMC Write/Read Level to Memory
DRQnn	DMC Request, Channel nn
ENDRG	End of Range
EOTBM	Output Bus to Address Counter (gating signal)
INBnn	Input Bus, Bits 1 to 16
IYBnn	Input to Y-register Bus, Bits 2 through 16 used by DMC Option and Program Interrupt
MCSET	Master Clock, Set Phase
MSTCL	Master Clear (Overall initialization)

Table 2 (Cont.)
Function Index

Mnemonic	Description
OTBnn	Output Bus, Bits 1 to 16
RRLIN	Reset Ready Line End of Range Line
TL1FF	Timing Level, TL1
TL2FF	Timing Level, TL2
TL3FF	Timing Level, TL3
TL4FF	Timing Level, TL4

Each channel has one DILXX line and one DALXX line. A device uses one of the DILXX lines to request a DMC cycle when it has data to input or is ready to accept data. The DMC will then send a break request to the CPU. When the CPU has completed the current instruction, a DMC cycle will be executed.

The DALXX lines are used to notify a device that its request has been honored and a DMC cycle is currently being executed.

The DMC executes an input if bit 1 of the starting address location is a ONE. An output is executed if bit 1 is a ZERO.

Bits 2 through 16 of the starting address specify a memory location where the data on the input bus will be stored when a DMC input is executed. The data in this location will be transferred to the device via the output bus when a DMC output is executed.

RRLIN is generated during each DMC cycle to notify the device that the data transfer is complete.

If the device is in the input mode, it uses DALXX to gate its data onto the input bus. If the device is in the output mode, it uses the coincidence of DALXX and RRLIN to strobe the data on the output bus into its buffer. Note that when in the output mode, the device must not gate data onto its input bus.

During each DMC cycle the contents of the starting address location will be increased by one. The first of the DMC transfers concerns the memory location initially stored in the starting address location. The second transfer concerns the next higher memory location, etc.

The terminal address is compared with the starting address during each DMC cycle. An end-of-range (ENDRG) signal is generated upon equality. The device may gate DALXX with ENDRG to inhibit further generation of requests. It may also generate an interrupt upon receipt of ENDRG.

Synchronization

Sync cycles occur when the DMC is not executing a DMC cycle. During this sync cycle, the DIL lines are interrogated. If a DIL is detected, a computer break is requested. When the computer completes the current instruction, a DMC cycle is initiated.

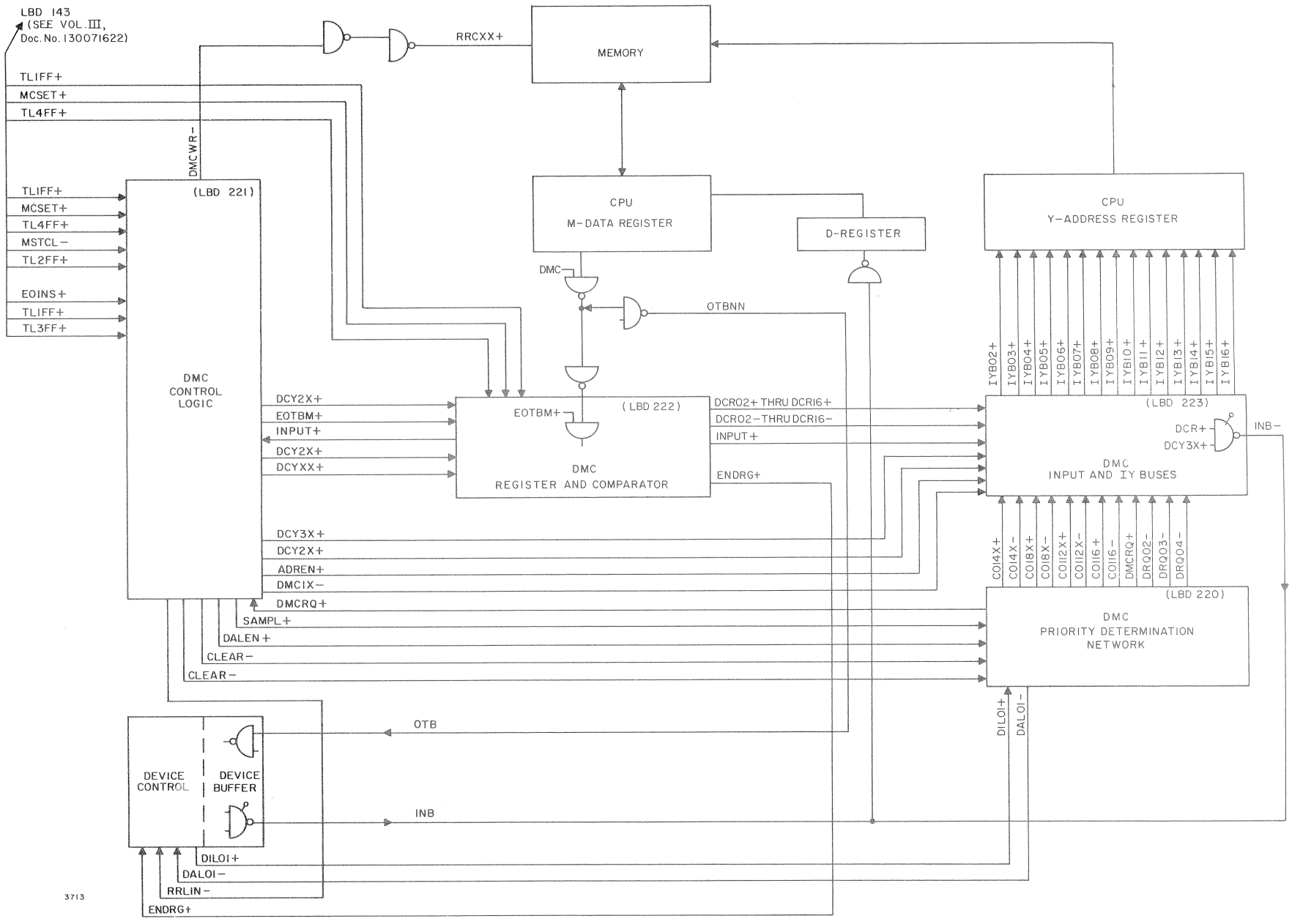


Figure 1. DMC Signal Interface Block Diagram

DMC Cycle

The DMC cycle requires four memory cycles.

The DMCWR flip-flop controls the direction of the four DMC memory cycles. When it is set, a write cycle is executed. When reset, a read cycle is executed.

The sequence of the DMC operations is controlled by the CPU master clock (LBD 118) and the DCYXX, DMC1X and DMC2X flip-flops (LBD 221). They are used to generate the four memory cycles shown in Figure 2.

The purpose of each memory cycle is as follows:

a. Fetch Starting Address. -- The contents of the starting address location are fetched and stored in the address counter register.

b. Fetch Terminal Address. -- The contents of the terminal address location are fetched and compared with the contents of the address counter register.

c. Data Transfer. -- The data transfer is controlled by the contents of the address counter register. If bit 1 is a ONE, an input is executed. If bit 1 is a ZERO, an output is executed. The contents of the address counter are increased by one.

d. Store Updated Starting Address. -- The contents of the address counter register are stored in the starting address location. If another DMC request is waiting, another DMC cycle starts. If no requests are waiting, the CPU resumes control.

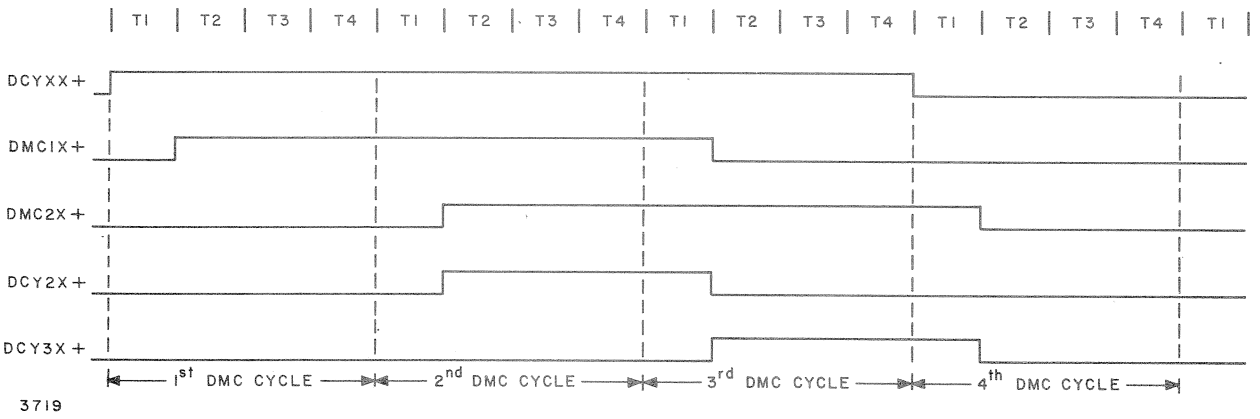


Figure 2. DMC Cycles

DETAILED ANALYSIS

Sync Cycle

The priority network is cleared by TL1FF of every sync cycle (CLEAR). SAMPL is generated by every TL2FF. If any DIL is true during SAMPL, the corresponding channel flip-flop in the priority network is set. (See Figure 3.) (Refer to the Appendix for the flow chart and analysis.)

When any of the channel flip-flops are set, the priority network (PN) notifies the CPU that a device has requested a DMC cycle by generating DMCRQ+. DMCRQ+ prepares the CPU for the execution of the DMC cycle by doing the following:

a. Inhibit all the transfer paths to the Y-Register other than the IY bus.
b. Inhibit PIL00 and SEX from using the IY bus.
c. Inhibit the setting of the fetch cycle flip-flop.

This allows the CPU to complete the current instruction; but prevents the starting of another instruction.

The priority network operates in a manner such that the highest priority channel flip-flop, of those which are set, enables the starting address location for that channel to appear on the IY bus. For example, if channel flip-flops 2, 7, and 9 are set, $(000022)_8$ will appear on the IY bus. SAMPL and CLEAR are inhibited until the end of the DMC cycle so that after having decided on priority and started the DMC cycle, the output of the priority network remains fixed.

EOINS is a level generated by the CPU which becomes true during the last cycle of each computer instruction. When DMCRQ, TL4FF and EOINS occur, the first DMC cycle is initiated.

First DMC Cycle

At DMCRQ · EOINS · TL4FF time, the IY bus is strobed into the Y-register. The DMCWR flip-flop is in the reset state, and MEMCI occurs. This set of conditions produces a memory cycle which fetches the contents of the starting address location and stores them in the M-register. (Refer to the Appendix for the flow chart and analysis.)

During the DMC cycle the contents of the M-register are gated to the output bus (LBD 138).

EOTBM+ (LBD 222) is used to strobe the contents of the output bus into the address counter register. This completes the fetch of the starting address.

Second DMC Cycle

The priority network continues to apply the starting address location to the IY bus. The terminal address location is always an odd number and one higher than the starting address (see table of addresses); therefore, bit 16 of the IY bus is changed from a ZERO to a ONE. This produces the terminal address location on the IY bus which is strobed into the

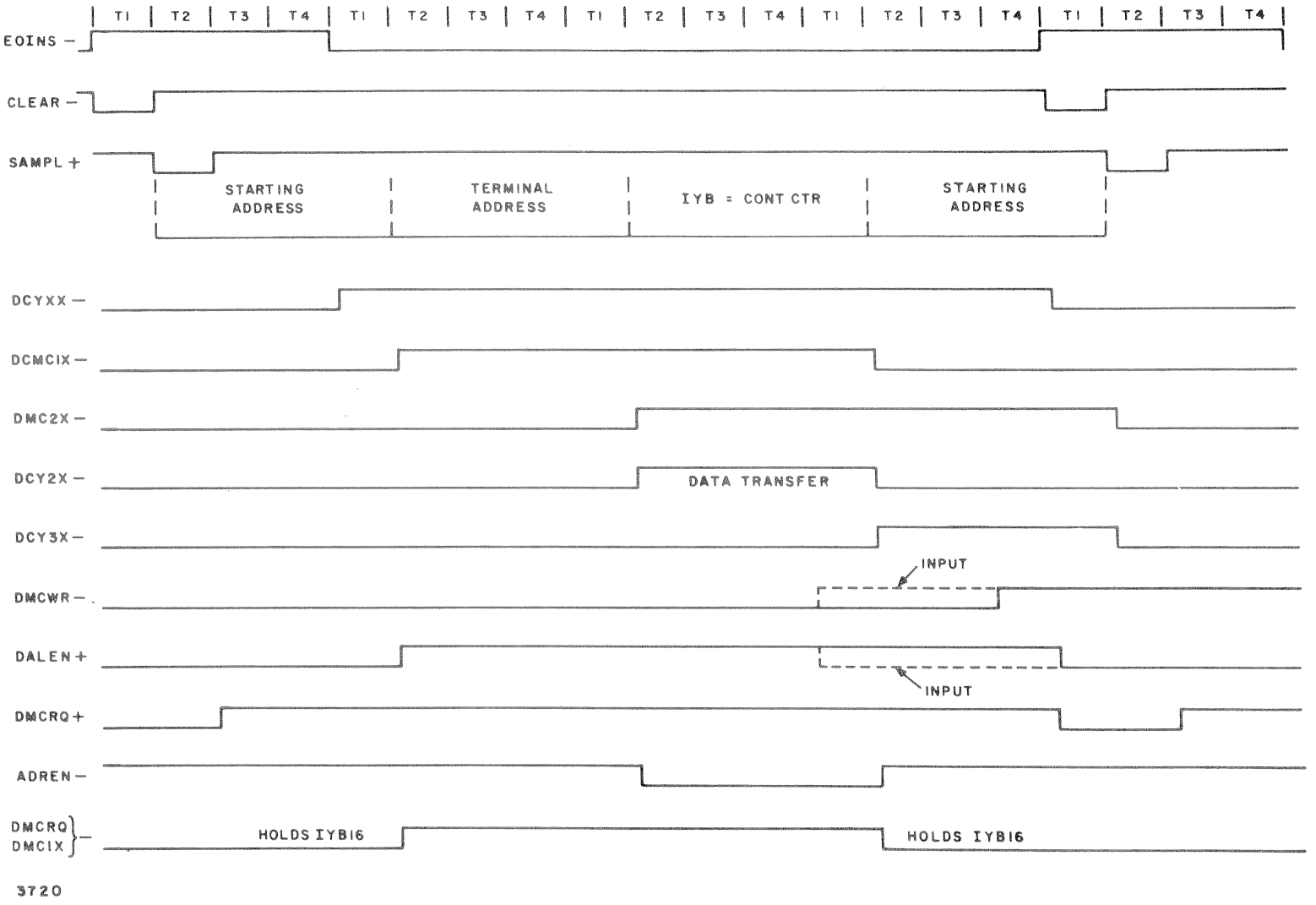


Figure 3. DMC Timing Cycle

Y-register at TL4FF time. Because DMCWR+ is still reset, the resulting memory cycle fetches the contents of the terminal address location which subsequently appears on the output bus. This address is compared with the starting address which is currently in the address counter. (Refer to the Appendix for the flow chart and analysis.)

The comparator (LBD 222) is a 15-bit exclusive OR network. The output is true if the 15 low order bits of the output bus are equal to the 15 low order bits of the address counter register, respectively.

ENDRG+ is generated if the output of the comparator is true.

The 15 low order bits of the address counter register will be transferred to the Y-register via the IY bus to provide the memory address of the third DMC cycle which performs the data transfer.

If bit 1 of the address counter register is set, an output transfer is called for and no further action takes place in the third DMC cycle.

If bit 1 of the address counter register is reset, an input transfer is called for and the following operations are carried out:

a. DMCRR (LBD 221) is sent to the CPU to generate RRLIN (LBD 134) indicating that the data on the input bus has been taken.

b. The contents of the input bus are strobed into the distribution D-register at TL3, and the contents of the D-register are strobed into the M-register at TL1.

c. The DMCWR flip-flop is set so that the following memory cycle writes the contents of the M-register into the memory.

d. The DALEN flip-flop is reset disabling all DAL lines and also clearing the input bus for use by the DMC.

Third DMC Cycle

In the output mode the contents of the memory location, specified by the 15 low order bits of the address counter register, appear on the output bus after TL2FF. RRLIN- (LBD 134) is generated by DMCRR (LBD 221). The device ANDs DALnn with RRLIN to strobe the contents at the output bus into its buffer. (Refer to the Appendix for the flow chart and analysis.)

The DALEN flip-flop is reset disabling all DAL lines.

For either input or output, the starting address is updated. The count pulse is generated (LBD 222) which adds one to the contents of the address counter register. The contents are then gated onto the input bus and strobed into the D-register. The DMCWR flip-flop is set so that this data is stored during the fourth DMC Cycle.

Fourth DMC Cycle

The contents of the D-register are transferred to the M-register to complete the operations necessary for updating the starting address. (Refer to the Appendix for the flow chart and analysis.)

The DCYXX flip-flop is reset, permitting the priority network to be cleared by the CLEAR pulse (LBD 221). TL2FF generates SAMPL. If any of the channel flip-flops are now set, DMCRQ is sent to the CPU, requesting another DMC cycle. EOINS is true during the fourth memory cycle of the DMC cycle; therefore, another DMC cycle can immediately follow. DMC cycles continue until all DIL lines are reset.

If no DIL lines are set, the contents of the P-register (program counter) are transferred to the Y-register, the DMCWR flip-flop is reset, and MEMCI initiates the fetch of the next instruction.

Special Wiring

All unused channels must be wired as shown on the following wiring chart.

Unused Channel Wiring Chart

Channel	From	Level	To	Level
1	A1C1203	1	A1C1213	1
2	A1C1205	1	A1C1223	1
3	A1C1210	1	A1C1211	1
4	A1C1216	1	A1C1230	1
5	A1C1303	1	A1C1313	1
6	A1C1305	1	A1C1323	1
7	A1C1310	1	A1C1311	1
8	A1C1316	1	A1C1330	1
9	A1C1403	1	A1C1413	1
10	A1C1405	1	A1C1423	1
11	A1C1410	1	A1C1411	1
12	A1C1416	1	A1C1430	1
13	A1C1503	1	A1C1513	1
14	A1C1505	1	A1C1523	1
15	A1C1510	1	A1C1511	1
16	A1C1516	1	A1C1530	1

PARTS LIST

The replaceable parts for the data multiplexed control option are listed in the following table. Component parts for the μ-PAC digital modules, unless stated otherwise in the listing, will be found in 3C Doc. No. 130071620.

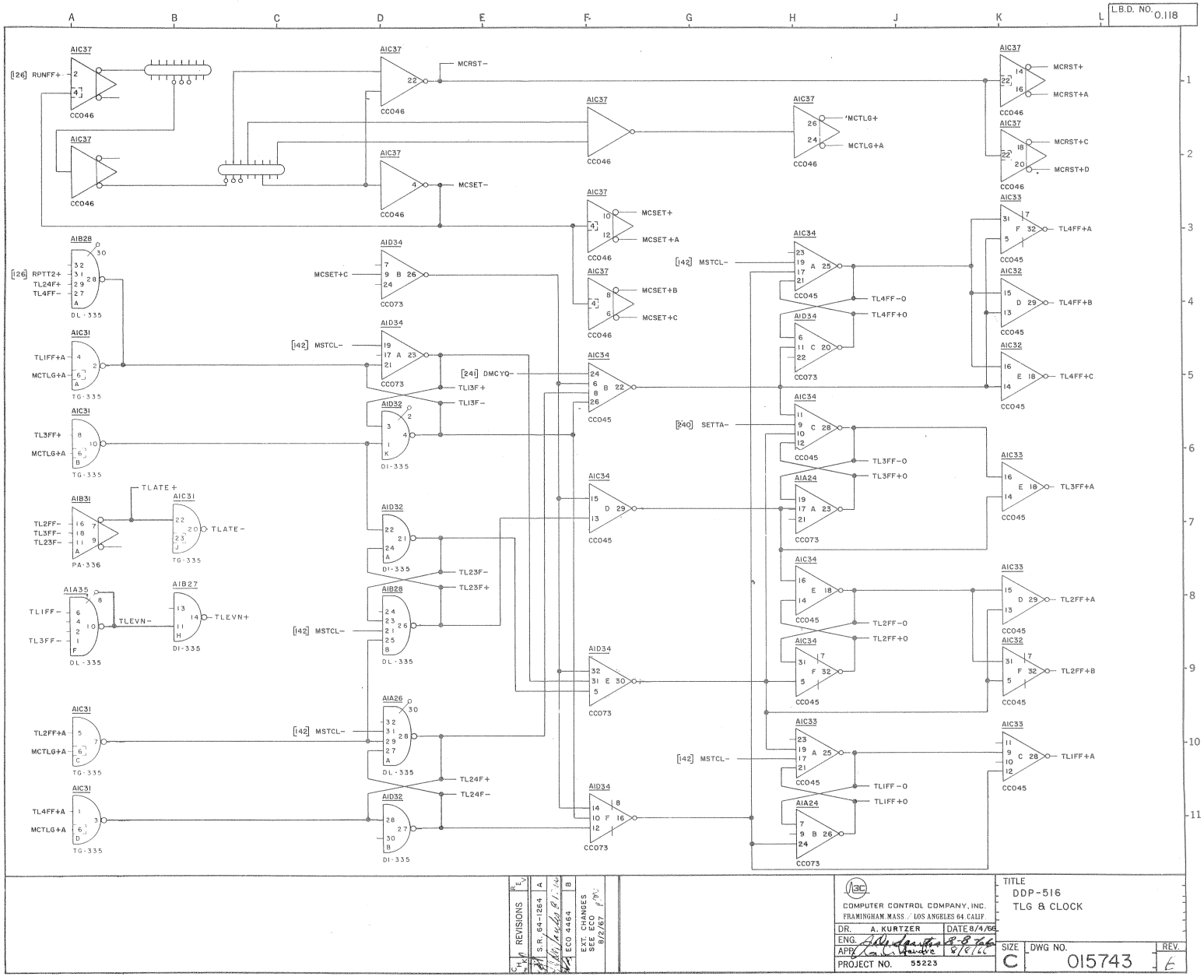
The reference (location) designations are in accordance with the DDP-516 coding drawings found in Volume III of 3C Doc. No. 130071620.

LOGIC BLOCK DIAGRAMS

Logic block diagrams for the DDP-516 DMC Option follow the parts list.

DDP-516 DMC Option Parts List

Reference Designation	Description	3C Part No.	Qty Req
	Channels 1 through 4		
A1C12	μ-PAC DIGITAL MODULE--priority PAC	Model CC-044	1
A1B12	μ-PAC DIGITAL MODULE--gated flip-flop	Model CC-089	1
A1C16, 17	μ-PAC DIGITAL MODULE--fast carry counter	Model CC-091	2
A1A12 A1D52	μ-PAC DIGITAL MODULE--parallel transfer gate	Model CC-022	2
A1B13, 15, 16	μ-PAC DIGITAL MODULE--selection gate Type 1; for component parts refer to Doc. No. 130071369	Model DG-335	3
A1A13, 16	μ-PAC DIGITAL MODULE--NAND gate Type 1	Model DI-335	2
A1A15	μ-PAC DIGITAL MODULE--NAND gate Type 2	Model DL-335	1
A1A14	μ-PAC DIGITAL MODULE--expandable NAND gate	Model DN-335	1
A1B17 A1B26	μ-PAC DIGITAL MODULE--power inverter	Model PA-336	2
A1A11 A1B14 A1B25 A1C18 A1C26	μ-PAC DIGITAL MODULE--transfer gate	Model TG-335	5
	Note: μ-PAC Model CC-054, reference designation A1C42, used in main frame logic (see Table 4-1, Vol. 1, Doc. No. 130071620), is to be removed when this option is made part of system configuration.		
	Channels 5 through 16		
	The following additional quantities of μ-PAC Model CC-044 are required for the channel groups as listed below:		
A1C13	Channels 5 through 8 1 required		
A1C13, 14	Channels 9 through 12 2 required		
A1C13, 14, 15	Channels 13 through 16 3 required		
A1A/B/C1	CONNECTOR PLANE ASSY--c/o one 1x3 connector block and associated parts; factory repairable only	3016018-701	1
A1B11 to Device A1C11 to Device A1A17 to Logic A1A18 to Logic	CABLE ASSY--four cables are required to interconnect the DMC option; type and part number will be specified by the system configuration		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DR. A. KURTZER DATE 8/4/66
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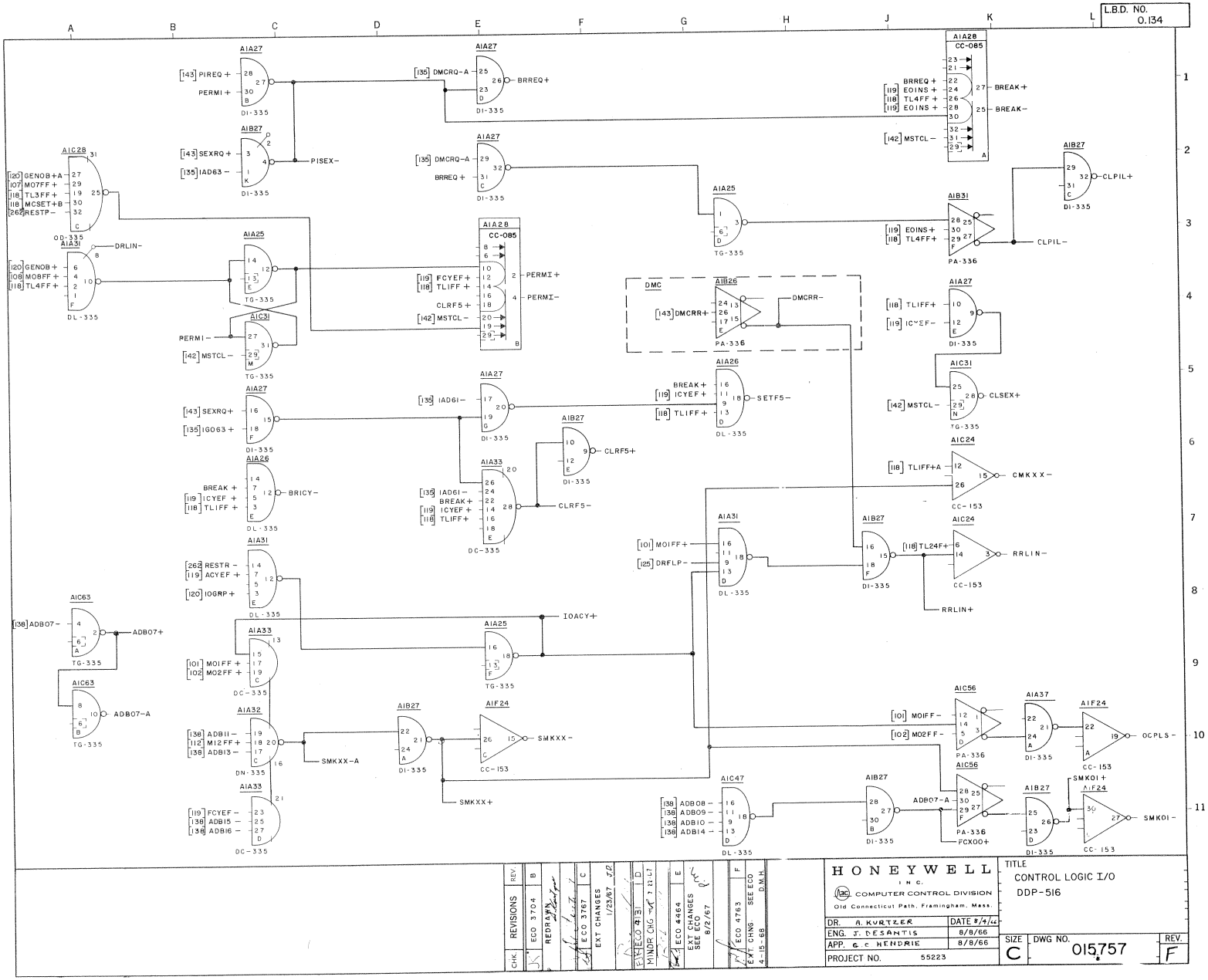
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HONEYWELL
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DR. A. KURTZER DATE 8/4/66
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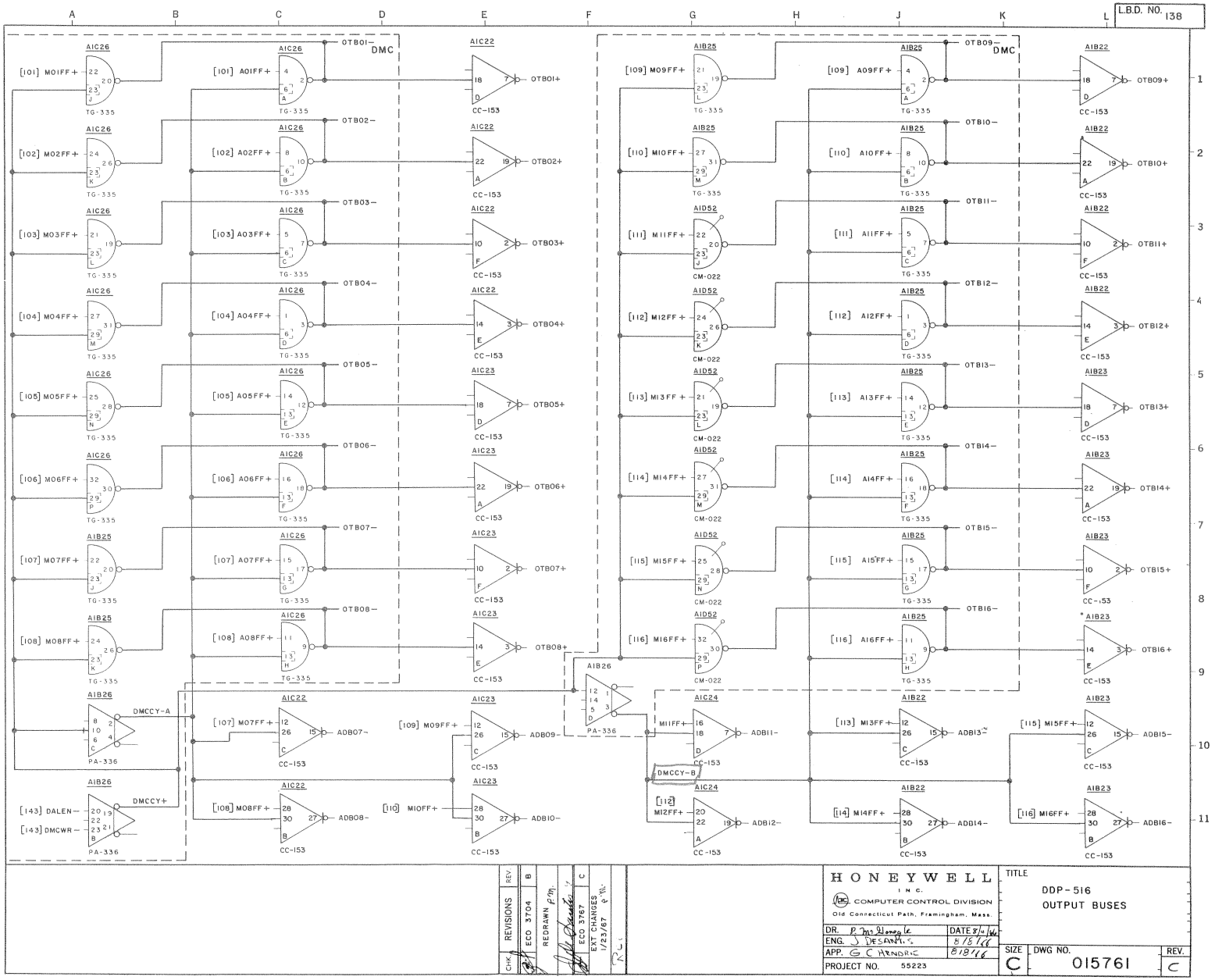
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Old Connecticut Path, Framingham, Mass.
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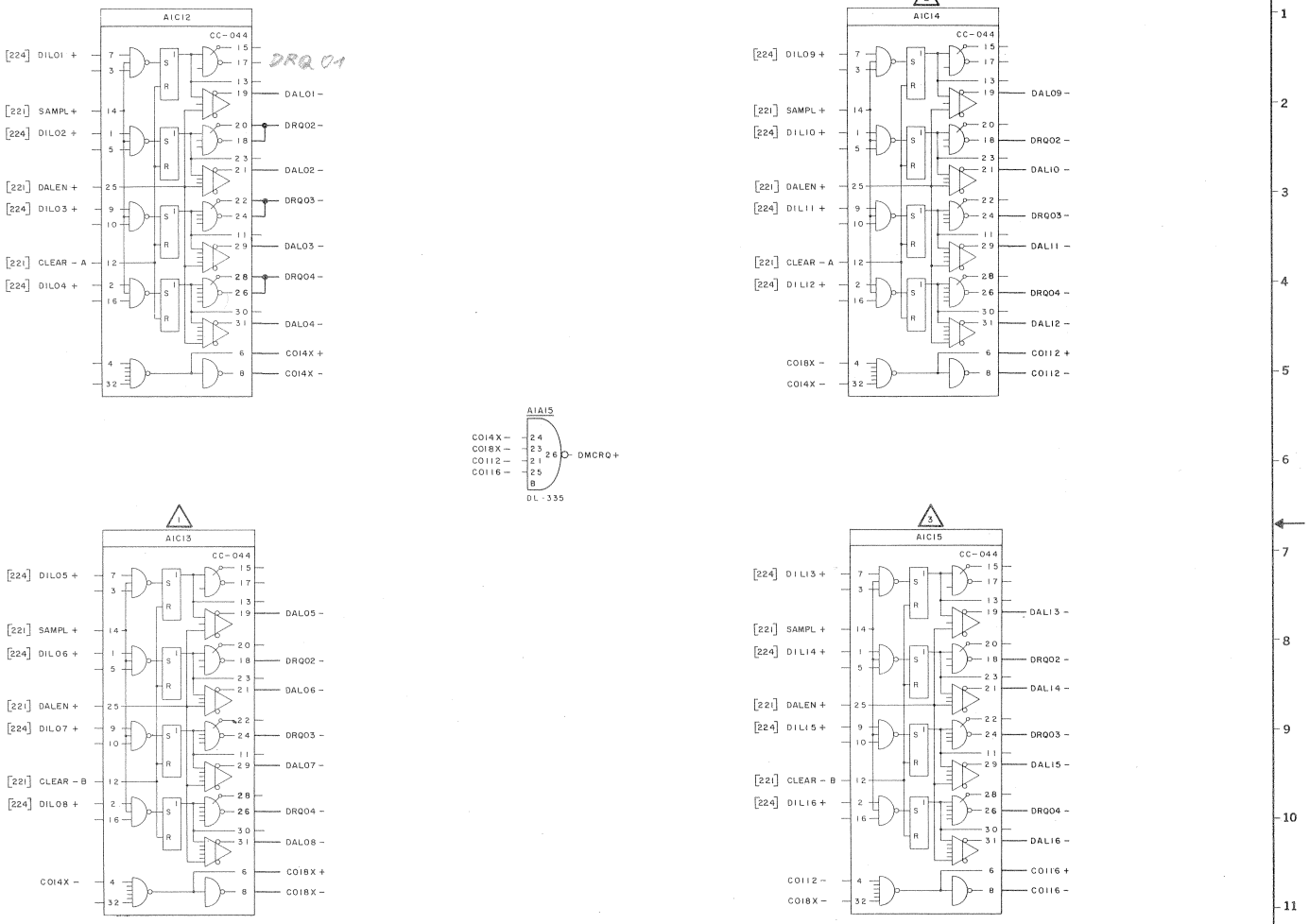
ENG. J. DESANTIS 8/5/66
APP. G C ANDRIC 8/8/66
PROJECT NO. 55223
TITLE
DDP-516
OUTPUT BUSES
SIZE C
DWG NO. 015761
REV. C

L.B.D. NO. 220



NOTES:

1. INSTALL IF MORE THAN 4 CHANNELS
2. INSTALL IF MORE THAN 8 CHANNELS
3. INSTALL IF MORE THAN 12 CHANNELS

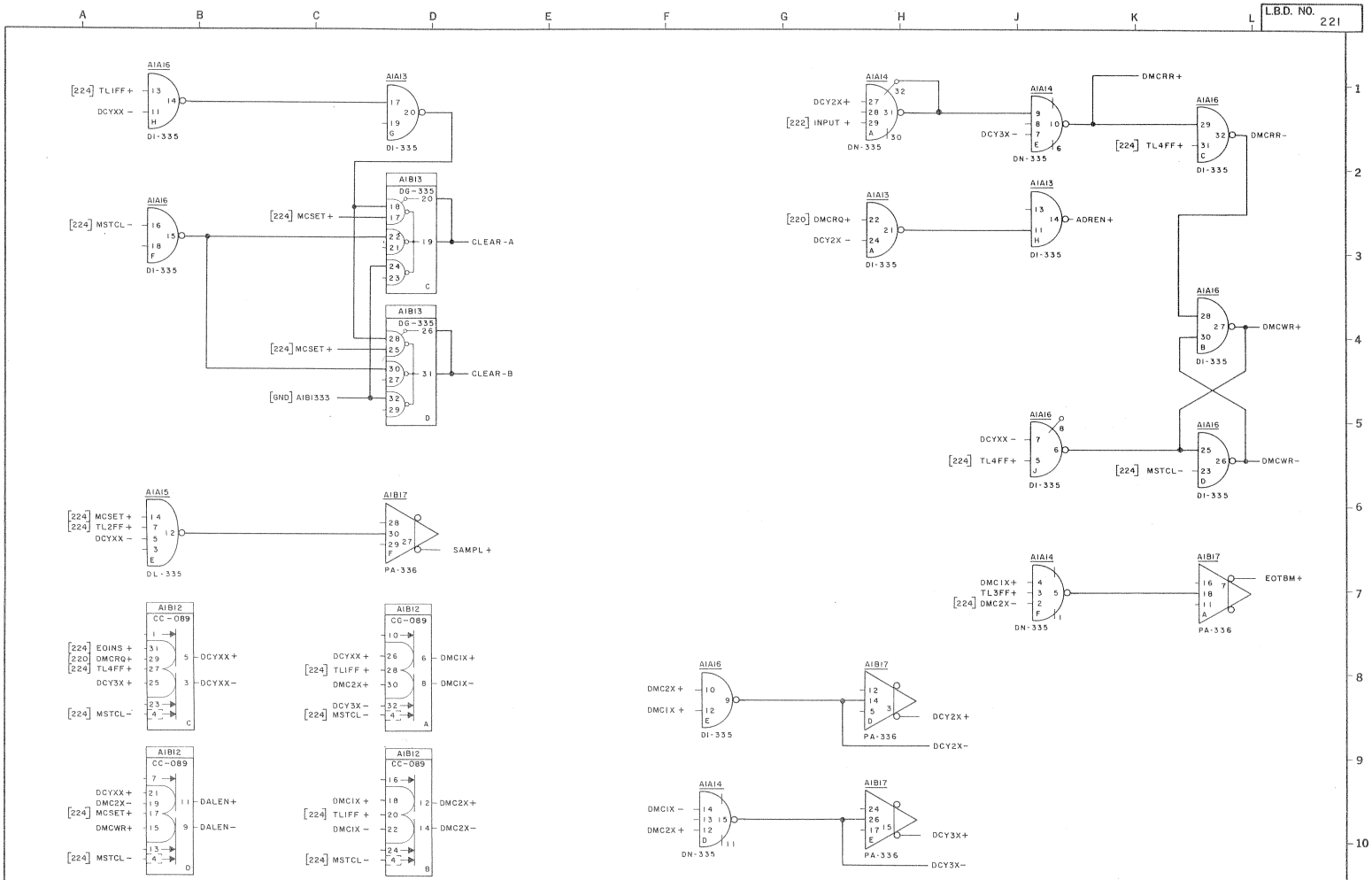
CHK	REVISIONS	REV.
	ECO #3902	B
	REDRAWN W/NO CHGS	

HONEYWELL INC.
COMPUTER CONTROL DIVISION
Old Connecticut Path, Framingham, Mass.

DR.	J. DOYLE	DATE
ENG.		10/4/66
APP.		11/15/66
PROJECT NO.	55215	

TITLE
DMC
PRIORITY
DETERMINATION NETWORK

SIZE	DWG NO.	REV.
C	016016	B



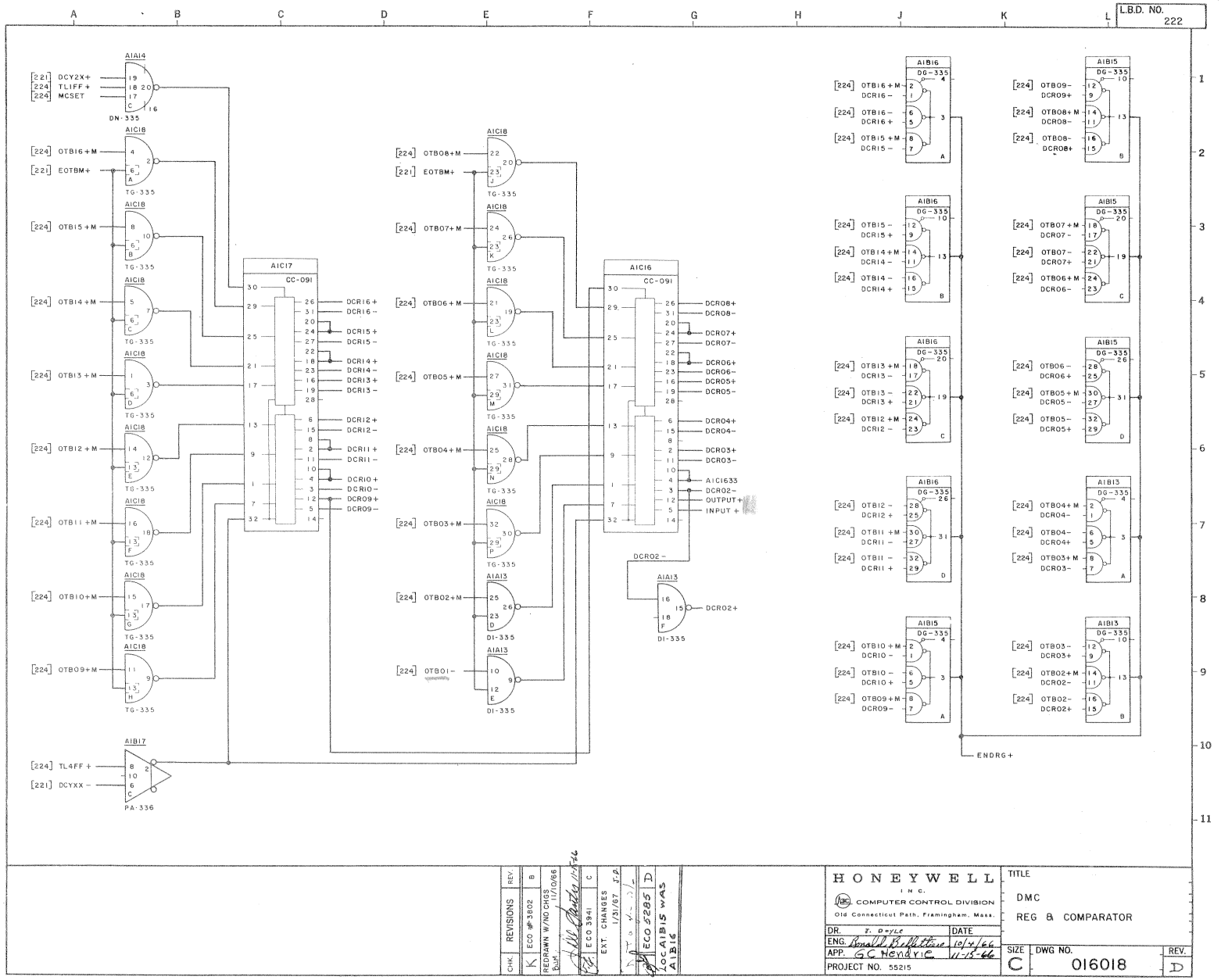
REV.	REVISIONS	CHK
B	ECO #3802 REDRAWN W/NO CHGS 11/10/66 B.S.M.	K
C	ECO 3941 EXT. CHANGES 11/31/67 S.P.	
D	ECO 4477 EXT. CHANGES JD 7/27/67	

HONEYWELL INC.
COMPUTER CONTROL DIVISION
Old Connecticut Path, Framingham, Mass.

DR. T. DOYLE	DATE	
ENG. Donald Bellerive	10/4/66	
APP. GC Hendrie	11-15-66	
PROJECT NO. 55215		

TITLE
DMC
CONTROL LOGIC

SIZE C | DWG NO. 016017 | REV. D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[224] MCSET
DN-335
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[224] OTB16+M
[221] EOTBM+
TG-335
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[224] OTB13+M
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DCR08-
DCR07+
DCR07-
DCR06+
DCR06-
DCR05+
DCR05-
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DCR03+
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DCR02-
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INPUT+
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DG-335
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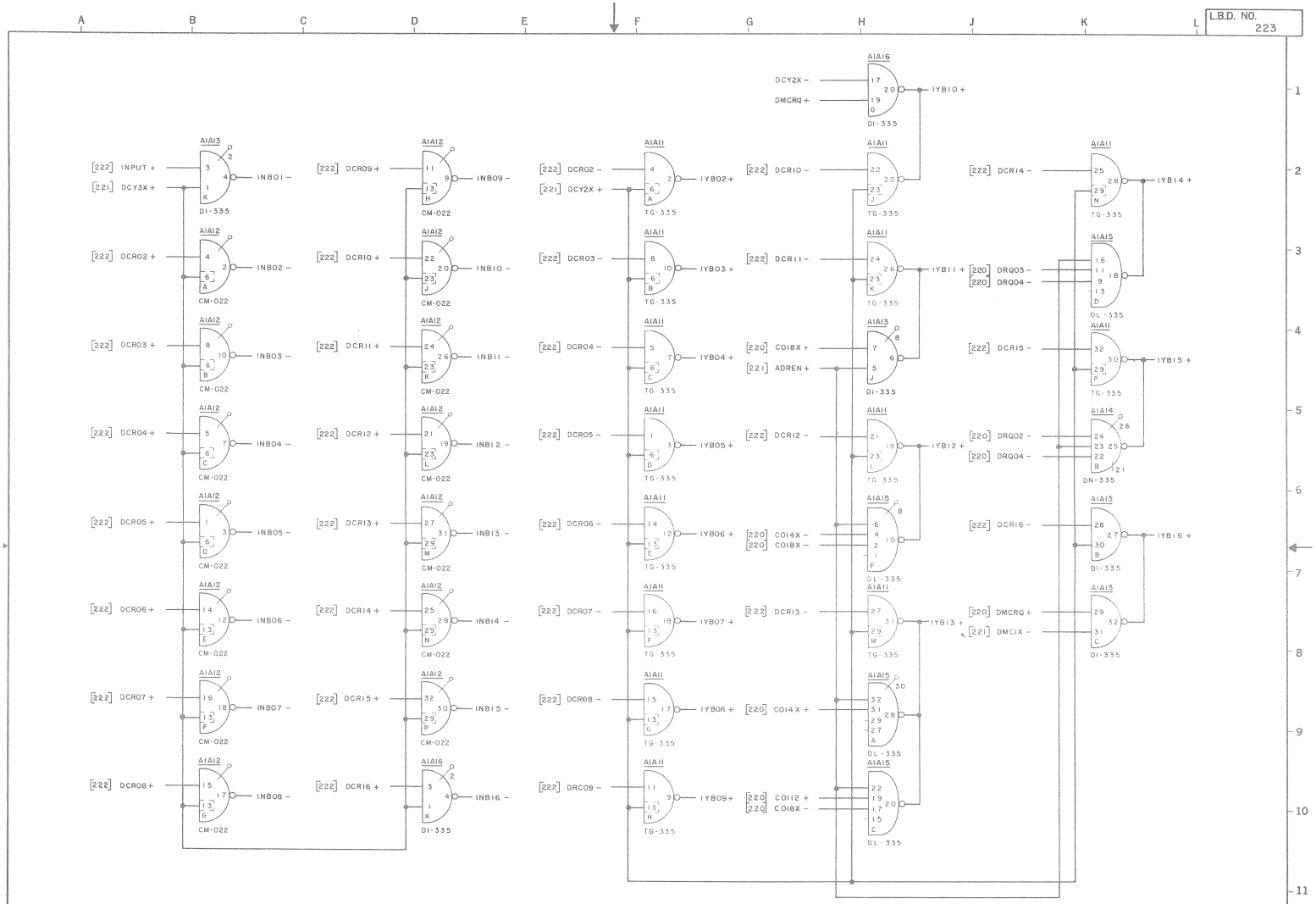
ENDRG+
REVISIONS
REV.
CHK
K ECO #3802 B
REDRAWN W/NO CHGS 11/10/66
ECO 3941 C
EXT. CHANGES 1/31/67 J.P.
ECO 5285 D
10CA1B15 WAS A1B16
HONEYWELL
INC.
COMPUTER CONTROL DIVISION
Old Connecticut Path, Framingham, Mass.
DR. J. Doyle DATE
ENG. Ronald Bellefleur 10/4/66
APP. GC Hendrie 11-15-66
PROJECT NO. 55215
TITLE
DMC
REG & COMPARATOR
SIZE C
DWG NO. 016018
REV. D



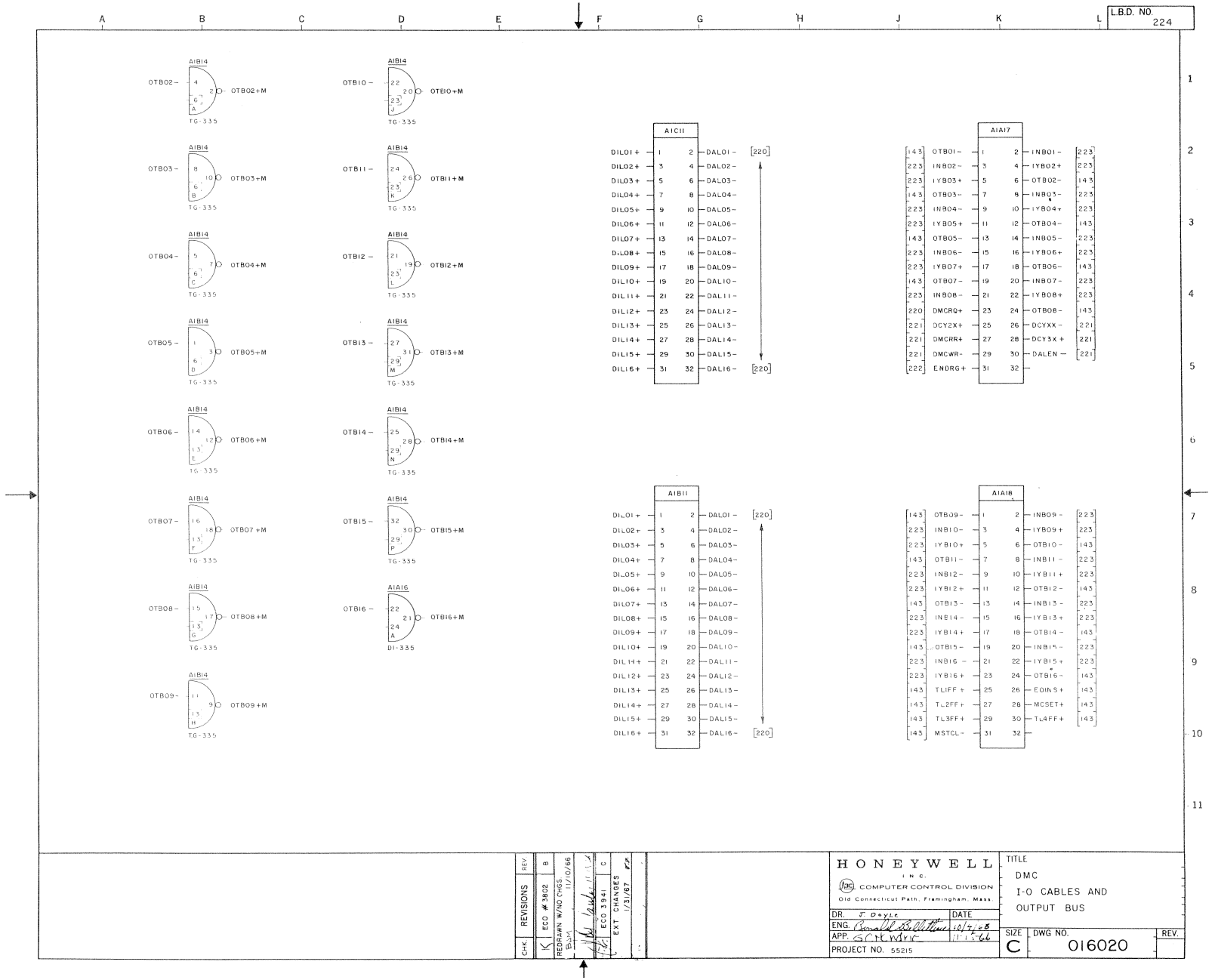
REVISIONS	REV.	ECO # 3802	REDRAWN W/NO CHGS D.J.M. 11/10/66
CHK.	B		

HONEYWELL INC.
COMPUTER CONTROL DIVISION
Old Connecticut Path, Framingham, Mass.

DR.	J. Doyle	DATE
ENG.		10/5/66
APP.		11/15/66
PROJECT NO.	55215	

TITLE
DMC
INPUT AND IY BUSES

SIZE	DWG NO.	REV.
C	016019	B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OTB02- 4 2 OTB02+M
6 7
A
TG-335
OTB03- 8 10 OTB03+M
6 8
B
OTB04- 5 7 OTB04+M
6 C
OTB05- 1 3 OTB05+M
6 D
OTB06- 14 12 OTB06+M
13 E
OTB07- 16 18 OTB07+M
13 F
OTB08- 15 17 OTB08+M
13 G
OTB09- 11 9 OTB09+M
13 H
OTB10- 22 20 OTB10+M
23 J
OTB11- 24 26 OTB11+M
23 K
OTB12- 21 19 OTB12+M
23 L
OTB13- 27 31 OTB13+M
29 M
OTB14- 25 28 OTB14+M
29 N
OTB15- 32 30 OTB15+M
29 P
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OTB16- 22 21 OTB16+M
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DI-335
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DIL02+ 3 4 DAL02-
DIL03+ 5 6 DAL03-
DIL04+ 7 8 DAL04-
DIL05+ 9 10 DAL05-
DIL06+ 11 12 DAL06-
DIL07+ 13 14 DAL07-
DIL08+ 15 16 DAL08-
DIL09+ 17 18 DAL09-
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DIL11+ 21 22 DAL11-
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DIL03+ 5 6 DAL03-
DIL04+ 7 8 DAL04-
DIL05+ 9 10 DAL05-
DIL06+ 11 12 DAL06-
DIL07+ 13 14 DAL07-
DIL08+ 15 16 DAL08-
DIL09+ 17 18 DAL09-
DIL10+ 19 20 DAL10-
DIL11+ 21 22 DAL11-
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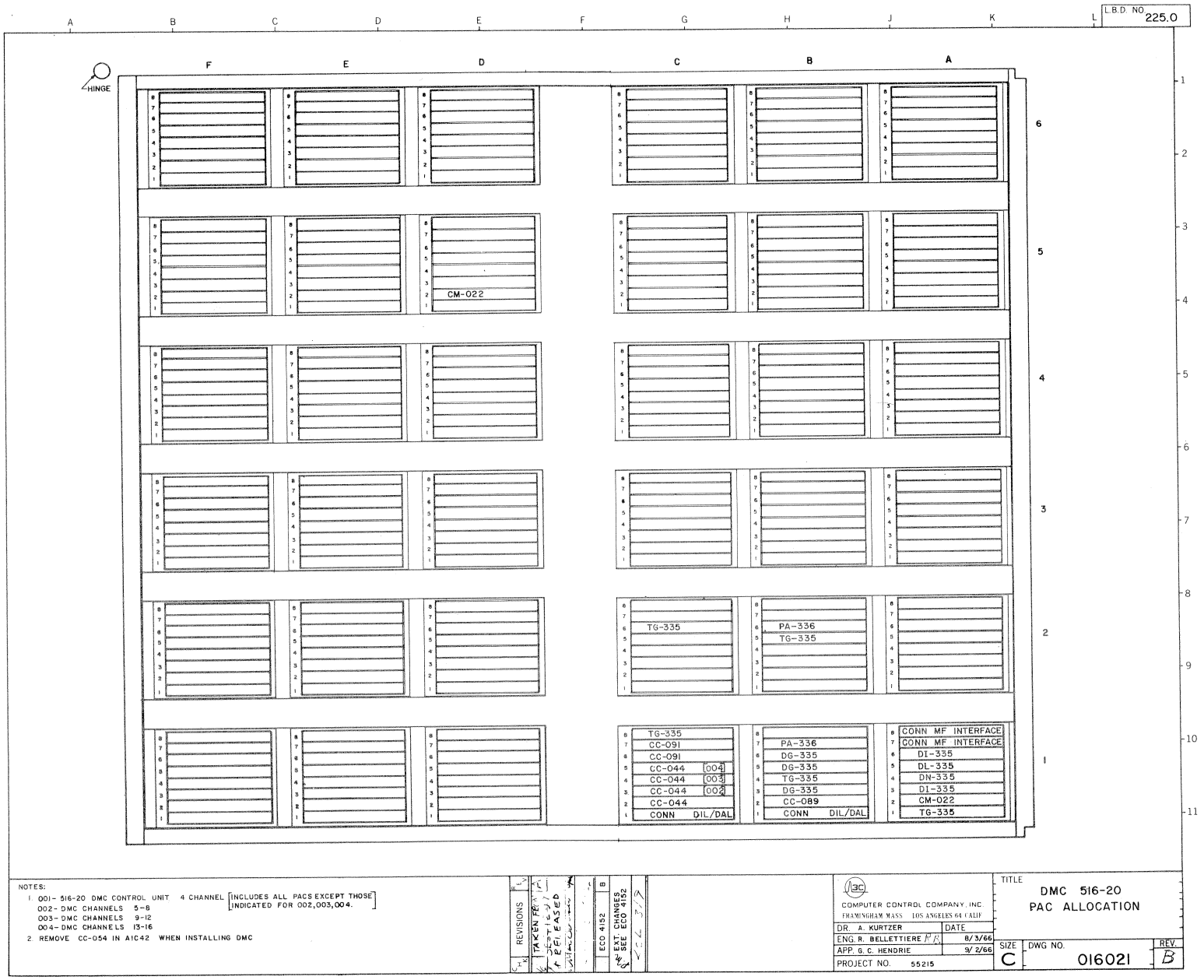
1 2 3 4 5 6 7 8 9 10 11
A B C D E F G H J K L
REVISIONS
REV
CHK
K ECO #3802 REDRAWN W/NO CHGS 11/10/66 B
ECO 3941 C
EXT. CHANGES 1/31/67
HONEYWELL
INC.
COMPUTER CONTROL DIVISION
Old Connecticut Path, Framingham, Mass.
DR. J Doyle
ENG. Ronald Bellefleur
APP. SCHWAYE
PROJECT NO. 55215
DATE 10/7/66
TITLE
DMC
I-O CABLES AND
OUTPUT BUS
SIZE C
DWG NO. 016020
REV.



NOTES:

1. 001- 516-20 DMC CONTROL UNIT 4 CHANNEL [INCLUDES ALL PACS EXCEPT THOSE INDICATED FOR 002,003,004.
   002- DMC CHANNELS 5-8
   003- DMC CHANNELS 9-12
   004- DMC CHANNELS 13-16
2. REMOVE CC-054 IN A1C42 WHEN INSTALLING DMC

REVISIONS

A	TAKEN FROM FIELD RELEASED	
B	ECO 4152	SEE ECO 4152 FOR EXT. CHANGES

COMPUTER CONTROL COMPANY, INC.
FRAMINGHAM MASS LOS ANGELES 64 CALIF

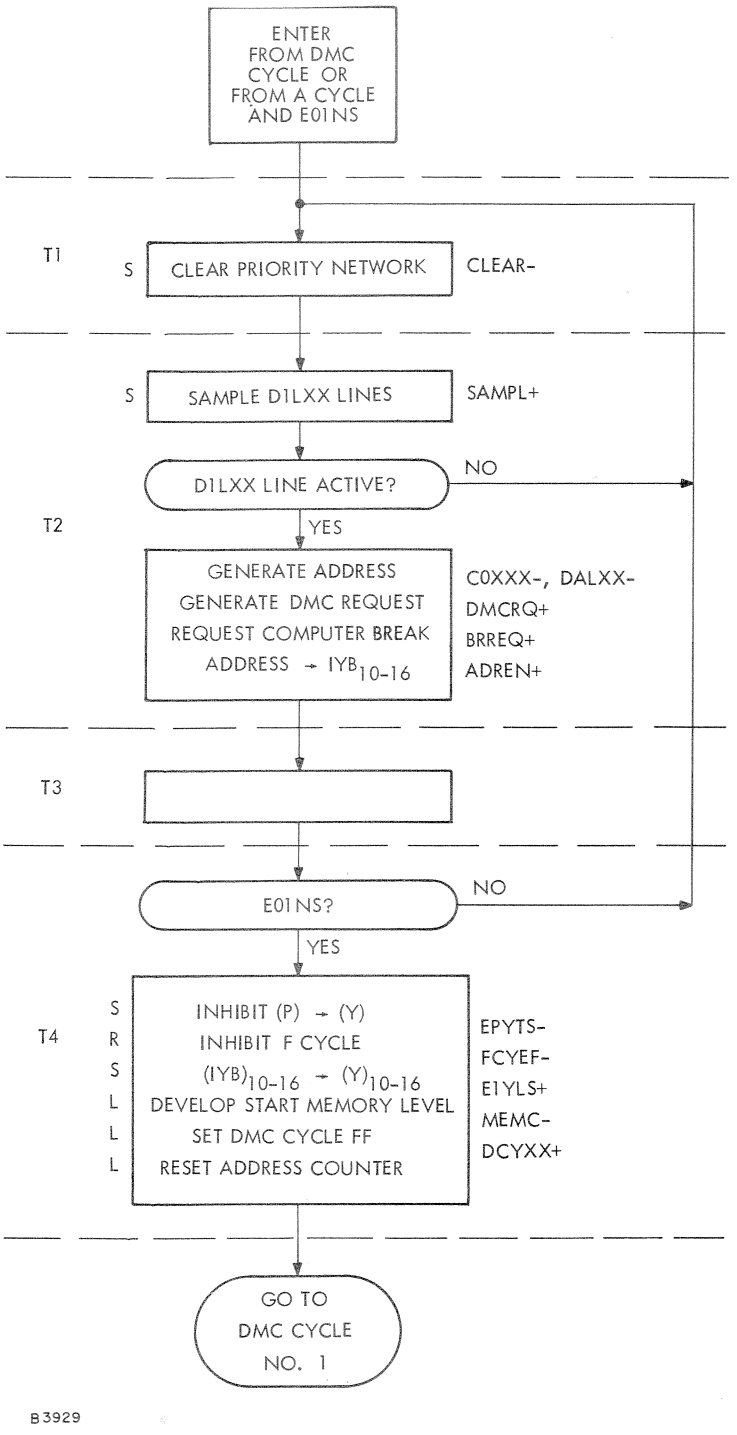
DR. A. KURTZER	DATE
ENG. R. BELLETTIERE	8/3/66
APP. G. C. HENDRIE	9/2/66
PROJECT NO. 55215	

TITLE
DMC 516-20
PAC ALLOCATION

SIZE C | DWG NO. 016021 | REV. B

APPENDIX
FLOW CHARTS AND ANALYSES

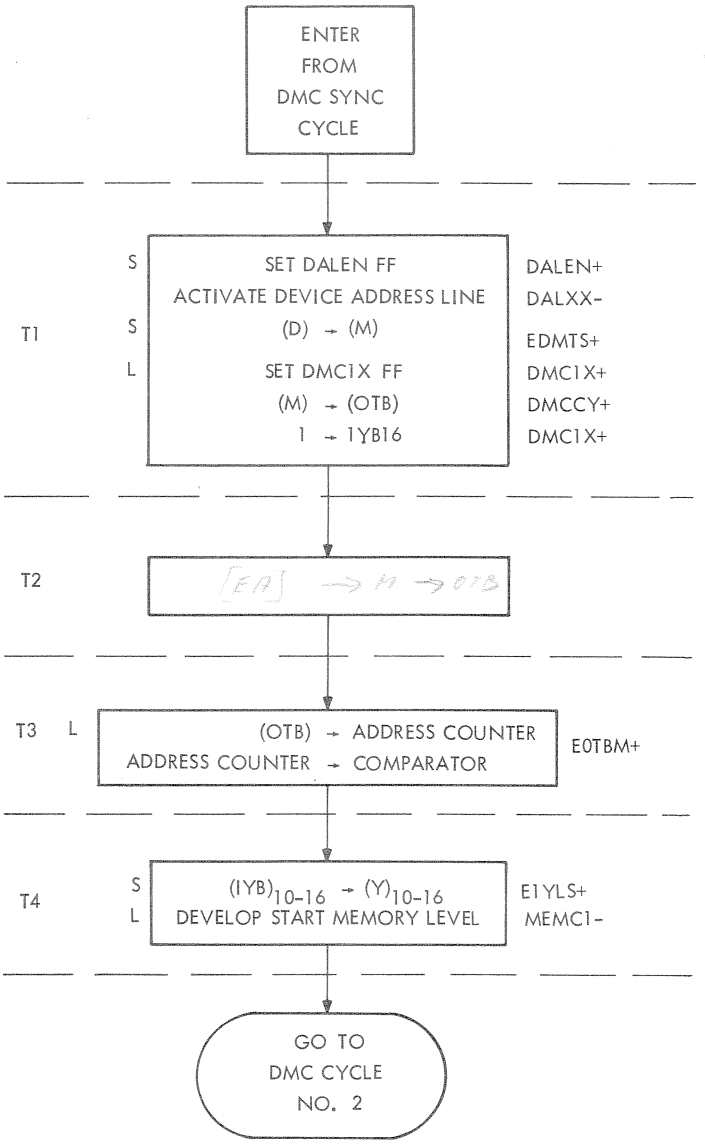
DMC Sync Cycle



DMC Sync Cycle

Signal	Origin	Cyc	Time	Clk	Signal Component	Origin	Destination	Operation Description
CLEAR-	221-D3		TL1	S	(DCYXX-)(TL1FF+)(MCSET+)	221-D4	220-B4/B10/ H4/H10	Clears PN
D1L01+ through D1L16+	External Device						220	Data transfer request to PN
SAMPL+	221-D7	F, I, or A	TL2	S	(DCYXX-)(MCSET+)(TL2FF+)	221-B7	220-B2/H2/ B8/H8	Enable active D1LXX requests to set associated PN channel flip-flops which generate DRQXX- and C0XXX- signals
C0XXX-	220-D51 D11/K5 K11				(SAMPL+)(D1LXX+)	220	220-F6 223-G/J	Generate DMCRQ+ Generate most significant portion of starting address location in 1YBXX+ lines
DRQXX-	220-D/K				(SAMPL+)(D1LXX+)	220	223-G/J	Generate most significant portion of starting address location on 1YBXX+ lines
DMCRQ+	220-F6				(C014X-)V(C013X-)V (C0112-)V(C0116-)	220-F6	119-D10 129-H4 134-E1 134-E2 135-F1 221-B9 221-F1 223-K7	Disables setting of FCYEF Disables P-register to Y-register Generates BRREQ+ Disables CLP1L Disables all devices other than DMC from using IY bus Enables set DCYXX FF (start DMC cycle) Enables ADREN+ Used to make 1YB16 ZERO when fetching starting address, as all starting address locations are even
BRREQ+	134-E1				(DMCRQ+)	134-E1	129-D5	Enables E1YLS+
ADREN+	221-H1				(DMCRQ+)(DCY2X-)	221-F1	223-H3	Enables PN address to IY bus
E1YLS+	129-L6		TL4	S	(BRREQ+)(E01NS+)(TL4FF+) (MCSET+)	129-D5	110--116-J10	Gates IY bus to P-register
MEMC1+	126-J11		TL4	L	(FCYLF-)(SPM0D-)(TL4FF+)	126-D11	150-C1	Initiates memory cycle
DCYXX+	221-B10		TL4	L	(DMCRQ-)(E01NS+)(TL4FF+)	221-B10	119-B1 129-D6 221-B1 221-B6 221-B8 221-D10 221-H2 222-A11	Inhibits E01NS+ Disable EDYTS+ (D-register to Y-register) and enables E1YLS+ Disables CLEAR- Disables SAMPL+ Enables set DMC1X FF Enables set DALEN FF Disables reset DMCWR FF Disables address counter common reset

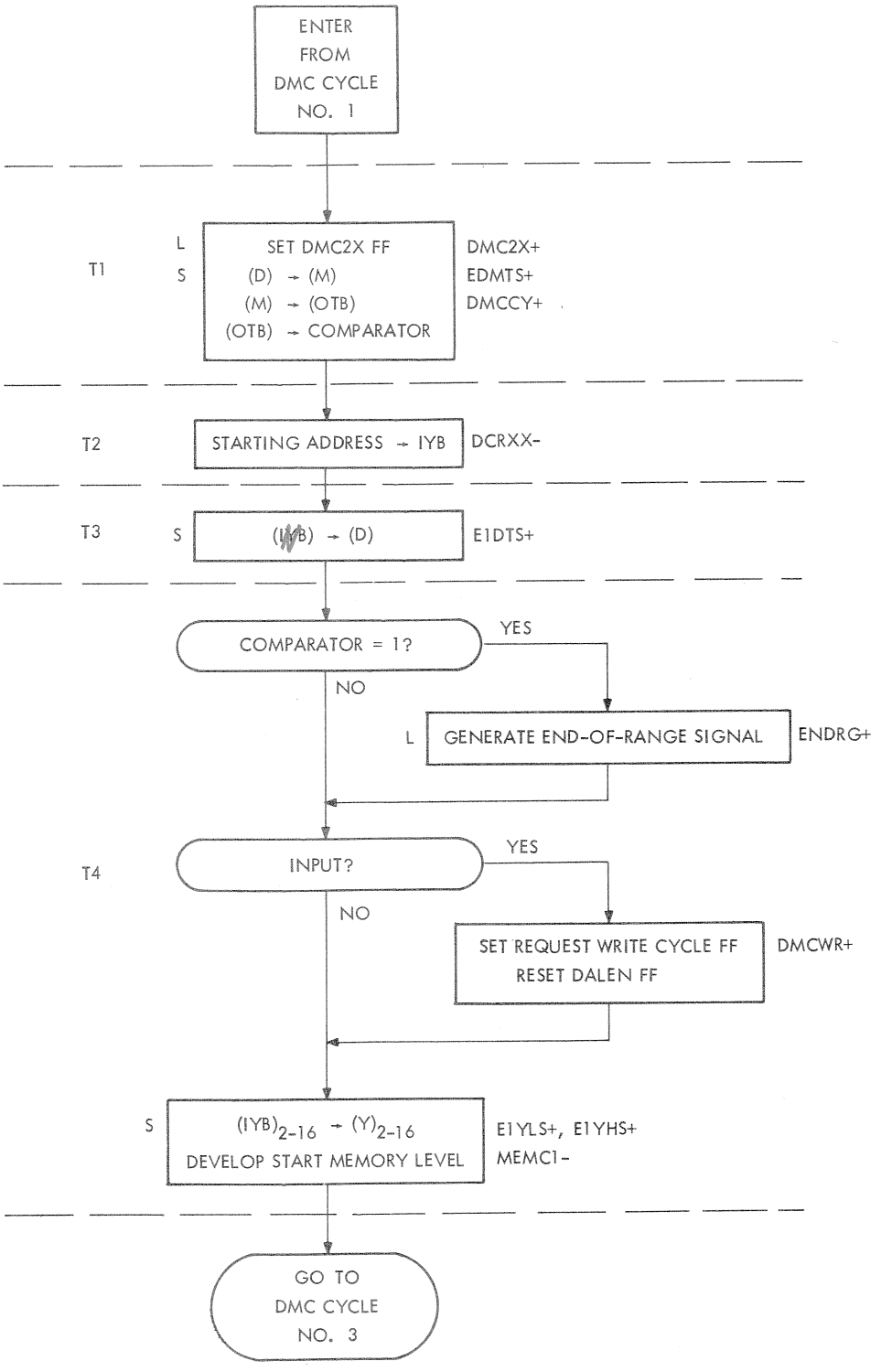
DMC Cycle No. 1



DMC Cycle No. 1

Signal	Origin	Cyc	Time	Clk	Signal Component	Origin	Destination	Operation Description
DALEN+	221-D10	DMC	TL1	S	(DCYXX+)(DMC2X-)(MCSET-)	221-D10	138-A11	Generates DMCCY+ which gates M-register contents to output bus
DALXX-	220				(DALEN+)(D1LXX+)	220	224-G	Device address lines
EDMTS+	128-K11	DMC	TL1	S	(0PGSM-)(RRCXX-)(MAST0-)	128-G11	101--116-G8	Clears M-register
DMC1X+	221-B8	DMC	TL1	L	(DCYXX+)(TL1FF+)	221-B8	221-D8 221-H3 221-H5 223-K7	Enables set DMC2X FF Enables DCY2X+ Disables DCY3X+ Puts a ONE on 1YB16+, as the final address is odd
E0TBM+	221-K6	DMC	TL3	L	(DMC2X)(TL3FF+)	221-H6	222-A2/B2	Gates OTB into address counter
E1YLS+	129-L6	DMC	TL4	S	(BRREQ+)(DCYXX+)(TL4FF+)	129-D5	110--116-J10	Gates IY bus to Y-register (starting address location +1 = final address location)
MEMC1+	126-J11	DMC	TL4	L	(FCYLF-)(SPM0D-)(TL4FF+)	126-D11	150-C1	Initiates memory cycle as DALEN+ is set, DMCCY+ gates the accessed starting address location to OTB

DMC Cycle No. 2

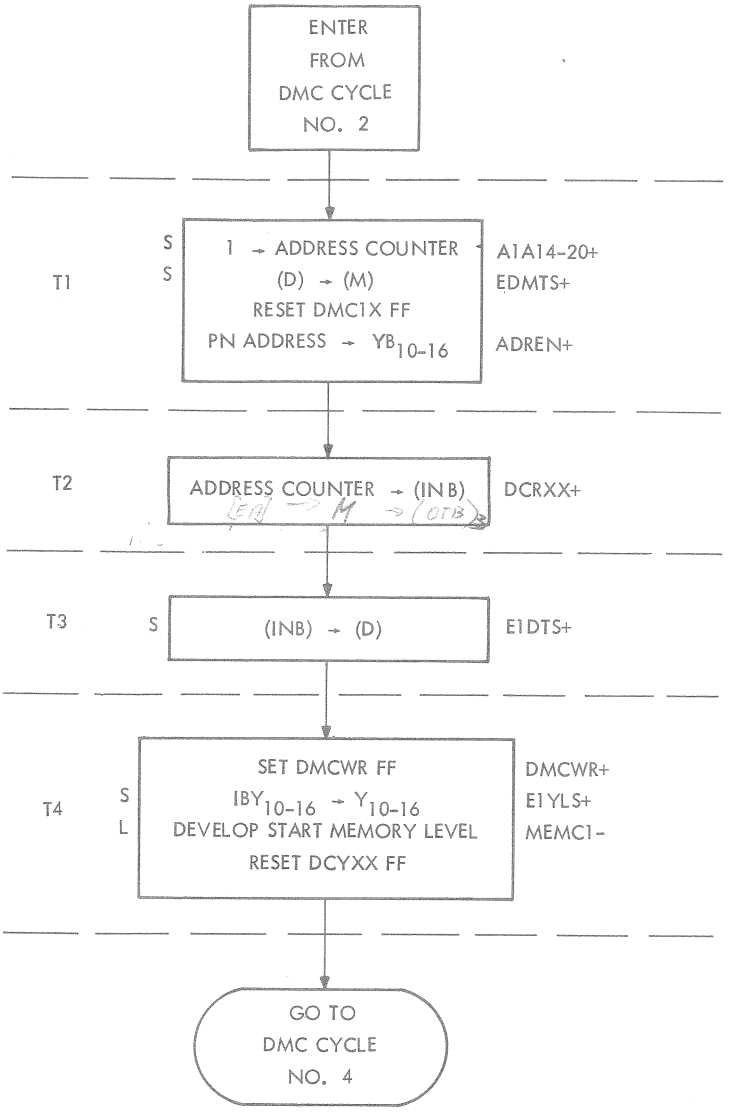


DMC Cycle No. 2

Signal	Origin	Cyc	Time	Clk	Signal Component	Origin	Destination	Operation Description
EDMTS+	128-K11	DMC	TL1	S	(0PGSM-)(RRCXX-)(MAST0-)(TL1FF1+)(MCSET+)	128-G11	101--116-G8	Clears M-register
DMC2X+	221-D8	DMC	TL1	L	(DMC1X+)(TL1FF+)	221-D8	221-B8 221-D10 221-H3 221-H5	Enable reset DMC1X FF Disable set DALEN FF Generates DCY2X+ Enables DCY3X+
DCY2X+	221-K4				(DMC1X+)(DMC2X+)	221-H4	129-H7 221-F2 221-F4 222-A1 223-F1	Enables E1YHS+ Disables ADREN+ If INPUT+, generates DMCRR+ Enables increment address counter Gates DCR02- through DCR16- to IY bus
DMCRR+	221-F5				(DCY2X+)(!INPUT+)	221-F4	134-G11 221-F2	Enables RRLIN+ Enables DMCRR+
RRLIN+	134-K8	DMC	TL24	L	(DMCRR+)(TL24F+)	134-G4/J6	125-H6	Enables E1DTS+
E1DTS+	125-L6	DMC	TL3	S	(RRLIN+)(TL3FF+)(MCSET+)	125-H6	101--116-D4	Gates input bus (external device data word) to D-register
DMCRR- DMCWR+	221-F2 221-K1	DMC	TL4	L	(DMCRR+)(TL4FF+) (DMCRR-)	225-F2 221-K1	222-K1 125-A5 126-H6 138-A11 221-D10	Set DMCWR FF Disables CLDTR- (clear D-register) Disable RRCXX+ to cause a write cycle Generates DMCCY+ to gate contents of M-register to output bus Resets DALEN FF
E1YLS+	129-L6	DMC	TL4	S	(BRREQ+)(DCYXX+)(TL4FF+)(MCSET+)	129-D5	110--116-J10	Gates IYB_{10-16} to Y_{10-16}
E1YHS+	129-L7	DMC	TL4	S	(BRREQ+)(DCYXX+)(DCY2X+)(TL4FF+)(MCSET+)	129-L7	102--109-J10	Gates IYB_{2-9} to Y_{2-9}
MEMC1+	126-J11	DMC	TL4	L	(FCYLF-)(SPM0D-)(TL4FF+)	126-D11	150-C1	Initiates memory cycle to readout or store data word

DMCCY LB138

DMC Cycle No. 3

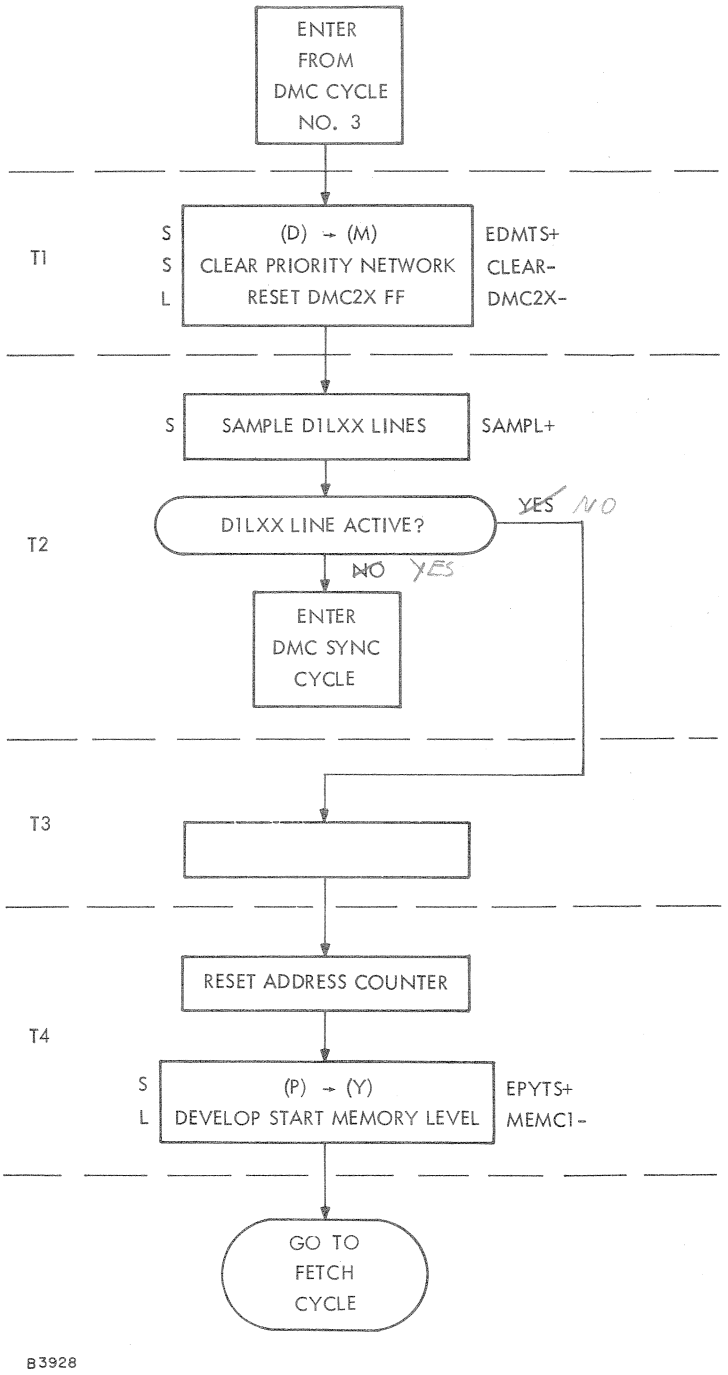


B 3926

DMC Cycle No. 3

Signal	Origin	Cyc	Time	Clk	Signal Component	Origin	Destination	Operation Description
A1A14-20+	222-A1	DMC	TL1	S	(DCY2X+)(TL1FF+)(MCSET+)	222-A1	222-C3	Increment address counter contents by 1
EDMTS+	128-K11	DMC	TL1	S	(0PGSM-)(RRCXX-)(MAST0-)(TL1FF+)(MCSET+)	128-G11	101--116-G8	Clears M-register
DMC1X-	221-B8	DMC	TL1	L	(DMC2X+)(TL1FF+)	221-B9	221-H3 221-H5	Disables DCY2X+ Generates DCY3X+
ADREN+	221-H1				(DMCRQ+)(DCY2X-)	221-F1	223-H3	Enables PN address to IY bus
DCY3X+	221-K5				(DMC1X-)(DMC2X+)	221-H5	221-B8 221-B10 221-F4 223-A1	Holds DMC1X FF reset Enables reset DCYXX FF Generates DMCRR+ Gates DCR01+ to 1NB01 (of 1NPUT+) and DCR02+ through DCR16+ to 1NB02 through 1NB16
DMCRR+	221-F4				(DCY3X-)	221-F4	134-G11 221-F2	Enables RRL1N+ Enables DMCRR-
RRL1N+	134-K8	DMC	TL24	L	(DMCRR+)(TL24FF+)	134-G4/J6	125-H6	Enables E1DTS+
E1DTS+	125-L6	DMC	TL3	S	(RRL1N+)(TL3FF+)(MCSET+)	125-H6	101--116-D4	Gates input bus (incremented starting address) to D-register
DMCRR-	221-G2	DMC	TL4	L	(DMCRR+)(TL4FF+)	221-F2	221-K1	Set DMCWR FF
DMCWR+	221-K1				(DMCRR-)	221-K1	125-A5 126-H6 138-A11 221-D10	Disables CLDTR- (clear D-register) Disables RRCXX+ to cause a write cycle Generates DMCCY+ to gate contents of M-register to output bus Resets DALEN FF
E1YLS+	129-L6	DMC	TL4	S	(BRREQ+)(DCYXX+)(TL4FF+)(MCSET+)	129-D5	110--116-J10	Gates IYB_{10-16} to Y_{10-16}
MEMC1+	126-J11	DMC	TL4	L	(FCYLF-)(SPM0D-)(TL4FF+)	126-D11	150-C1	Initiates memory cycle to store incremented starting address
DCYXX-	221-B10	DMC	TL4	L	(DCY3X+)(TL4FF+)	221-B10	119-D1 221-B1 221-B6 221-H2 222-A11	Enable E01NS- Enables CLEAR- Enables SAMPL+ Enables reset DMCWR FF Enables address counter common reset

DMC Cycle No. 4



DMC Cycle No. 4

Signal	Origin	Cyc	Time	Clk	Signal Component	Origin	Destination	Operation Description
EDMTS+	128-K11	DMC	TL1	S	(0RGSM-)(RRCXX-)(MAST0-)(TL1FF+)(MCSET+)	128-G11	101--116-G8	Gates contents of D-register into M-register
CLEAR-	221-D3/D4	DMC	TL1	S	(DCYXX-)(TL1FF+)(MCSET+)	221-E3/E4	220-B4/B10/H4/H10	Resets PN channel flip-flops which disables DMCRQ+
DMC2X-	221-D8	DMC	TL1	L	(DMC1X-)(TL1FF+)	221-D8	221-K5	Disables DCY3+
SAMPL+	221-D6	DMC	TL2	S	(DCYXX-)(TL2FF+)(MCSET+)	221-B6	220-B2/B8/H2/H8	Enables active D1LXX requests to set associated PN channel flip-flops
A1B17-2-	222-A11	DMC	TL4	L	(DCYXX-)(TL4FF+)	222-A11	222-C7/G7	Reset address counter